Crystal®

Data Acquisition Products

Application Seminar

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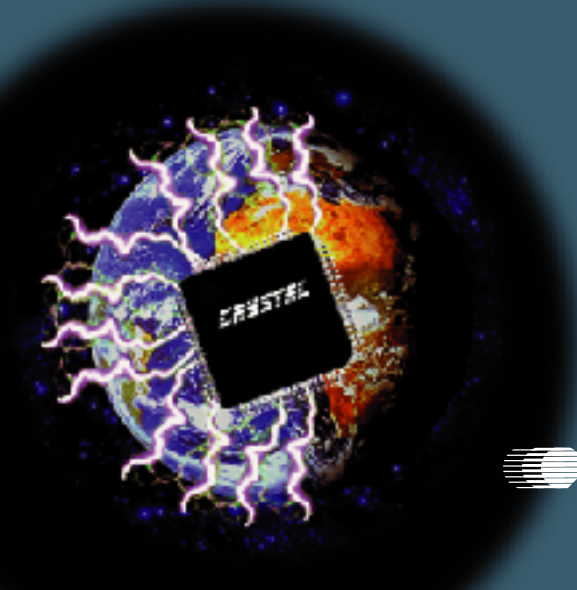

CIRRUS LOGIC®

CRYSTAL
MIXED-SIGNAL SOLUTIONS
FROM CIRRUS LOGIC

Crystal® Data Acquisition Products Applications Reference Guide

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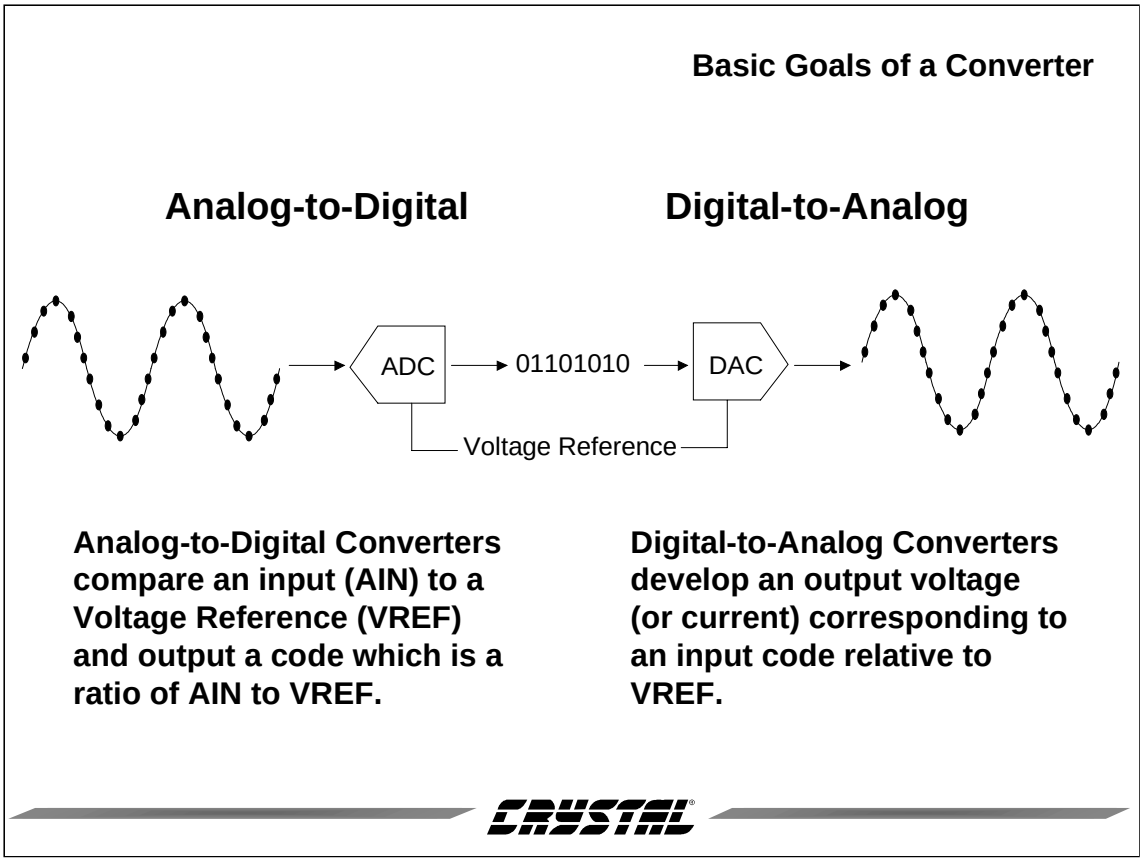
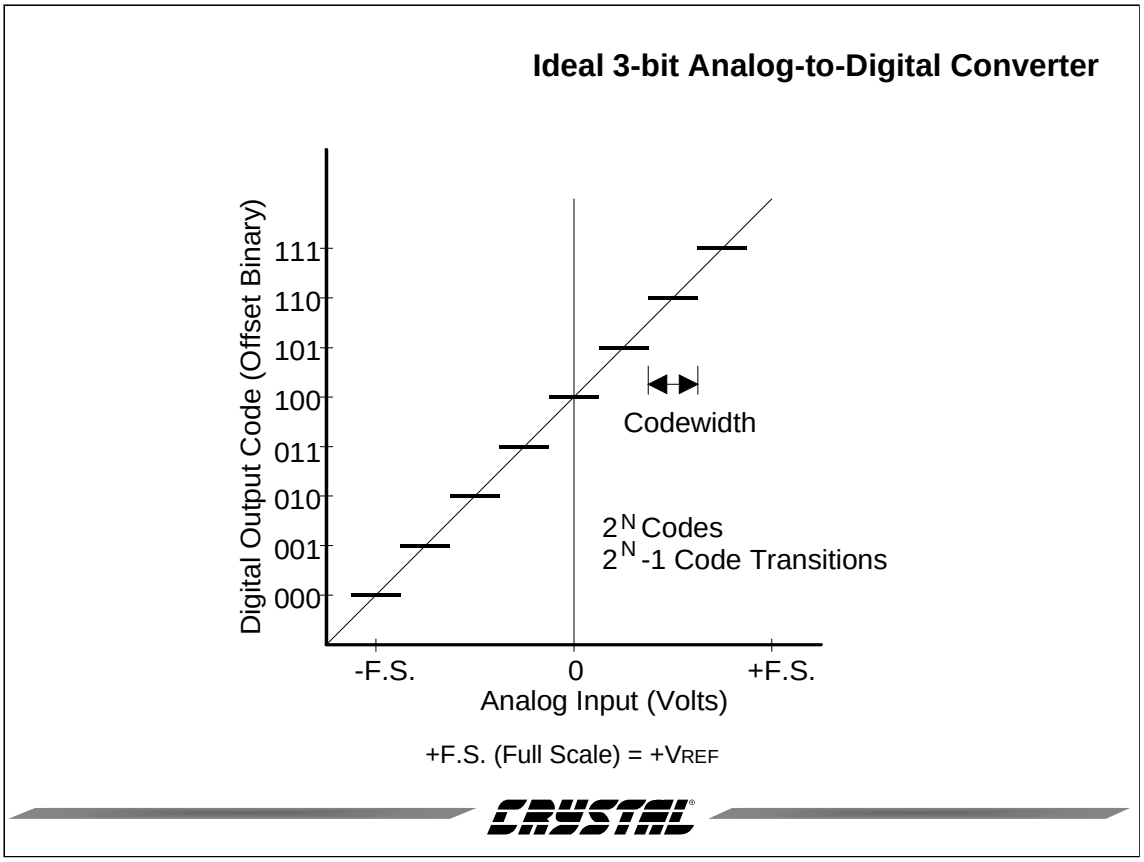
Applications Reference Guide - Section I

- **Introduction to Analog-to-Digital Converters**
- **Analog-to-Digital Converter Topologies**
- **Measurement, Testing and Troubleshooting**
- **DAQ ADC Applications Examples**
- **Technical Support Services**

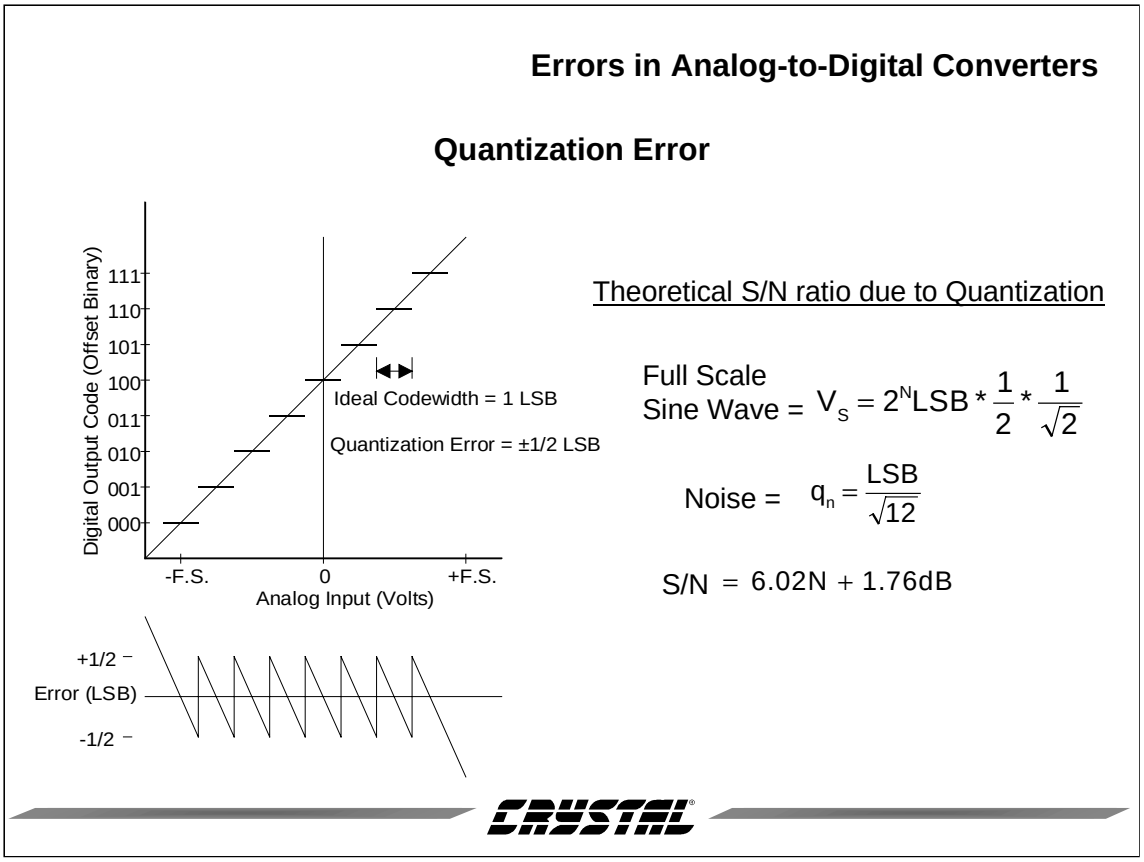


The goal of an Analog-to-Digital Converter is to generate a digital word which is representative of the magnitude of an analog signal. The goal of a Digital-to-Analog converter is to generate an analog signal which is representative of a digital word.



An Analog-to-Digital Converter (ADC) is a quantizer. It maps a continuously changing analog signal into discrete steps which are each represented by a digital code. This enables the signal to be stored or processed in digital form. The discrete steps represent a fixed portion of the value of the voltage reference being used.

An ADC has 2^Ncodes, N being the number of bits in the converter. Usual practice is to define the center of one of the codes as the zero point of the converter. By definition this means that a bipolar converter will have one fewer code on one half of the transfer function than the other. Thus, the full scale output code actually describes a point 1 Least Significant Bit (LSB) less than the value of the voltage reference.



Since an Analog-to-Digital Converter (ADC) is a quantizing device, it exhibits quantization error. Even an ideal ADC exhibits quantization error. Once an analog signal has been digitized, the digital code represents a specific analog value which may differ from the actual analog signal by as much as ± 1/2 LSB.

An ideal ADC has a theoretical S/N ratio which is defined by the ratio of a full scale root mean squared (rms) sine wave to the rms noise which results from quantization. This ratio results in the simplified equation: S/N = 6.02 N + 1.76 dB (N being the number of bits in the converter).

How Large is a Count/LSB

Analog-to-Digital Conversion with Full Scale = ±3V

$$\frac{6\text{Volts}}{2^{N}\text{Codes}}$$

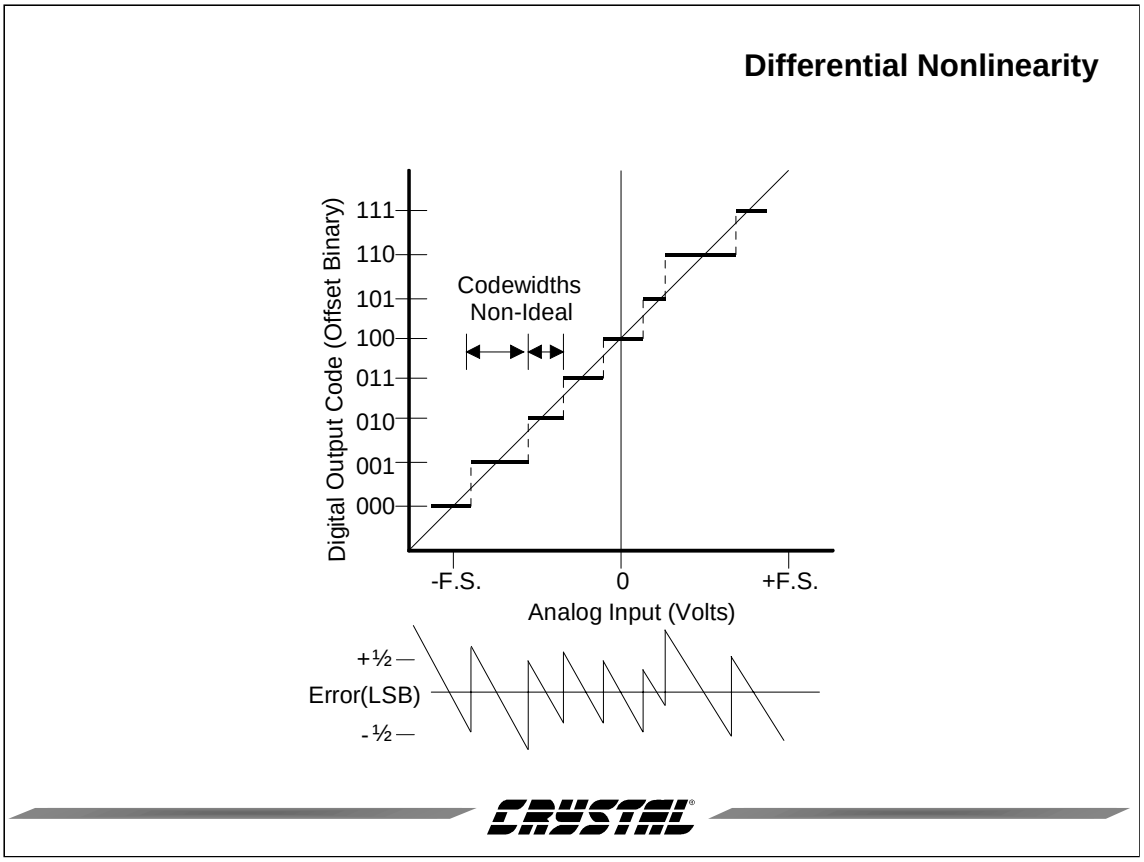
N =	**12**	**16**	**20**	**24**
1 Count or LSB =	**1.46 mV**	**91.5 μV**	**5.7 μV**	**0.36 μV**

Since each code of the converter represents a small portion of the total input voltage, it is helpful to examine just how much analog voltage a code in a converter actually represents. Imagine an example where the Full Scale signal to be measured is at 3 volts. For various converter resolutions, 12 to 24 bits, one LSB (also called one count) of the converter will represent a specific amount of voltage. For converters with 16 bits or greater, the voltage represented by one LSB is getting small relative to potential error sources in the circuit, such as noise and thermal drift.

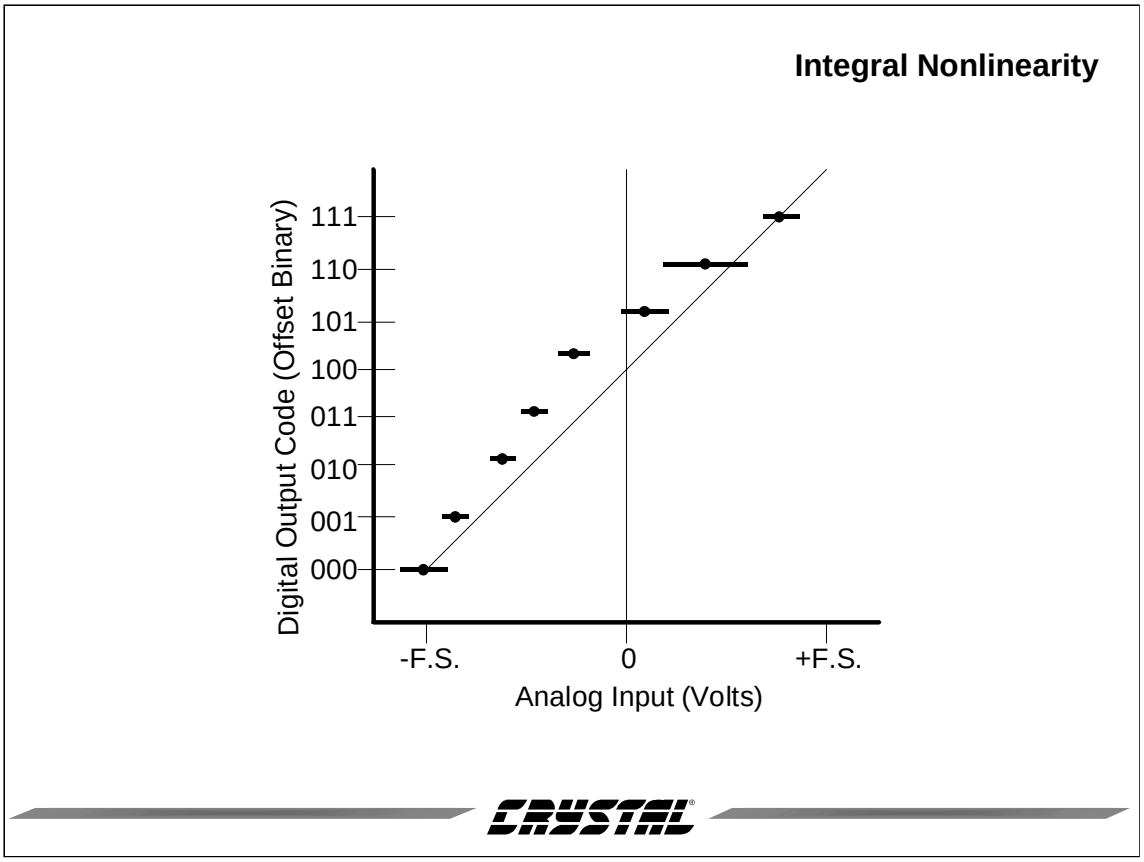
Ideal Analog-to-Digital Measurement
Resolution Signal to Noise

Analog-to-Digital N Bits	# of Codes	Resolution	Ideal S/N
12	4096	244 ppm	74 dB
16	65536	15 ppm	98 dB
20	1,048,576	0.95 ppm	122 dB
24	16,777,216	0.06 ppm	146 dB

The number of bits in an ideal converter determines its resolution and its ideal signal/noise ratio. Resolution defines the smallest portion of the full scale signal which can be resolved. Signal/noise ratio defines the ratio of a full scale root mean squared (rms) sine wave to the rms noise. Resolution and S/N can be each be improved by using a converter with more bits.

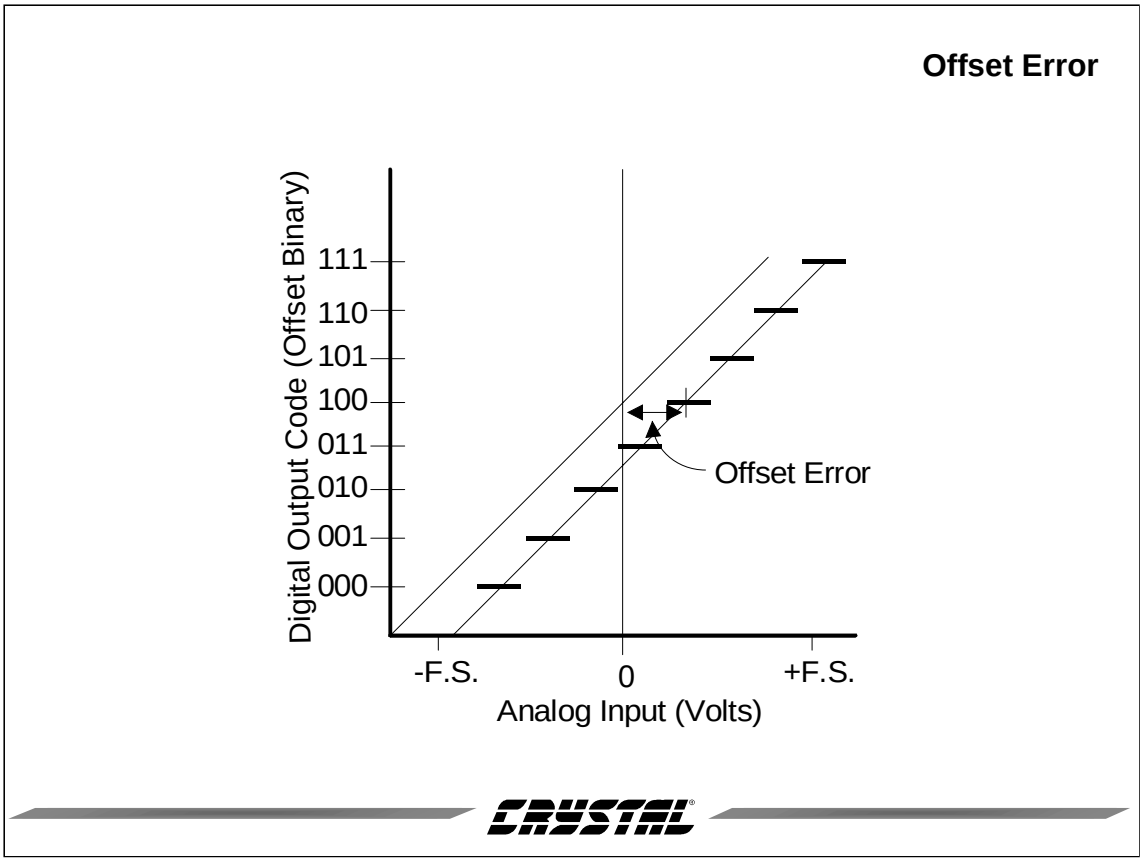


In a "real-world" Analog-to-Digital Converter the quantization step sizes can be larger or smaller than the ideal. This introduces an additional error called differential nonlinearity (DNL). DNL is a measure of the actual size of a code versus the ideal. Greater differential nonlinearity will tend to reduce the effective signal/noise of a converter. Variation in code sizes is largely determined by the matching accuracy of the elements which make up the converter. Large mismatches can result in very wide or very narrow codes, and can even result in missing codes in some converter architectures.

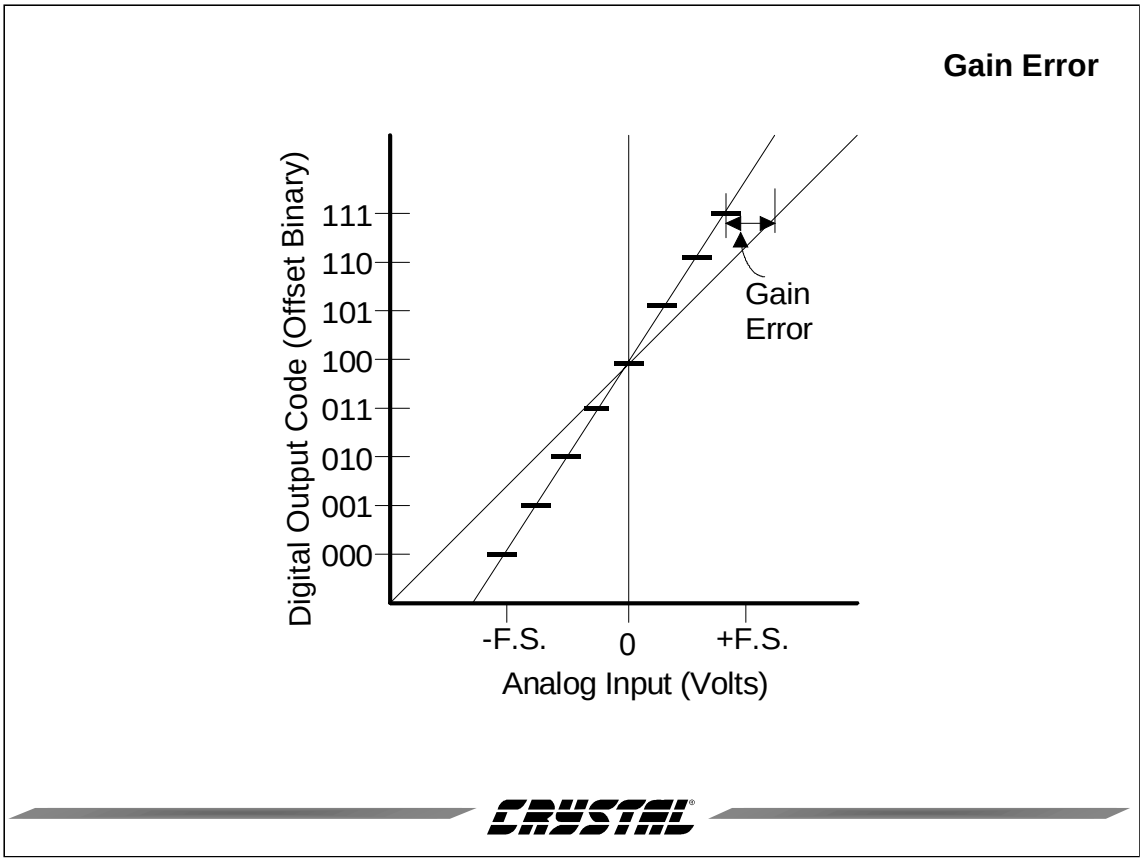


Integral Nonlinearity (INL) (also called integral linearity error) is a measure of the linearity of the entire transfer function. The method of measurement for integral nonlinearity can vary between manufacturers. Cirrus uses an "endpoint linearity" definition in which a straight line is drawn between the codes at each end of the transfer function. Integral nonlinearity is the measure of the distance from this line to the center point of the code which lies the farthest distance from the line. Some manufacturers use a "best fit" straight line method which yields an optimistic measure of linearity.

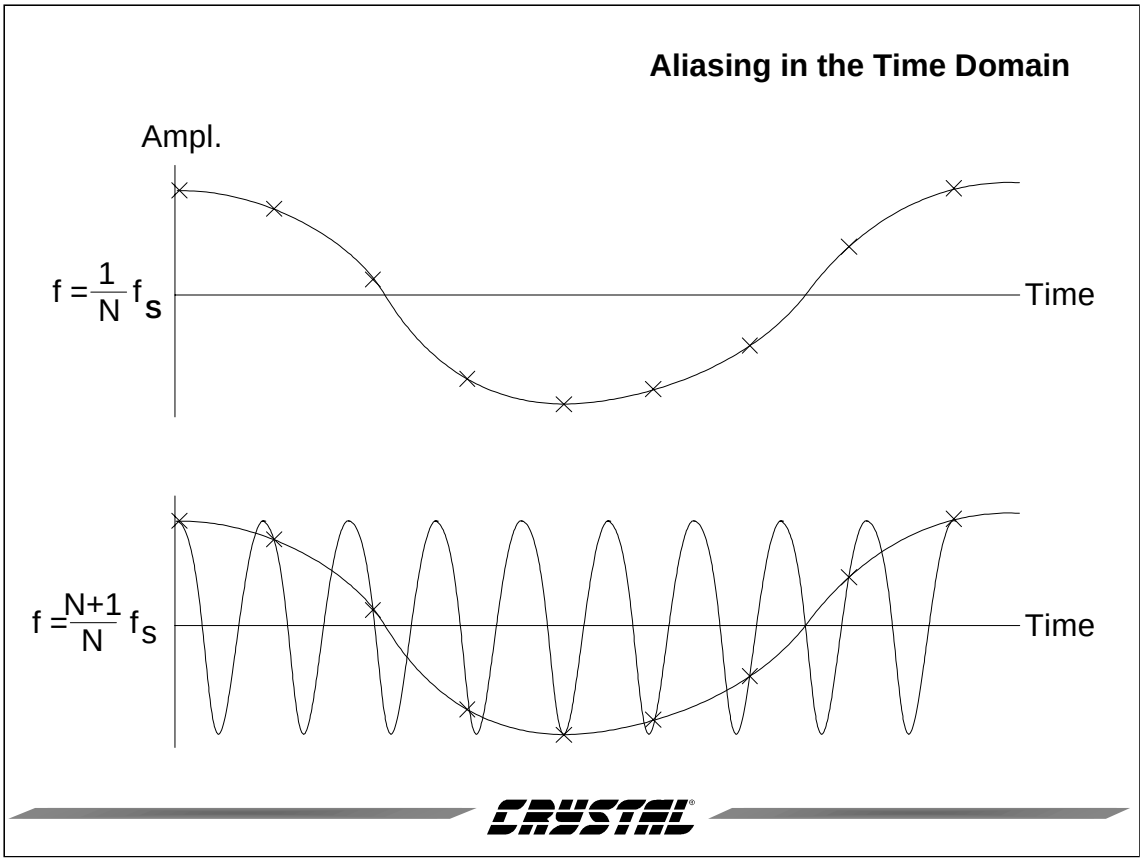
The integral nonlinearity specification is commonly found on Analog-to-Digital Converter (ADC) data sheets for converters intended for instrumentation applications. In spectral measurement or signal processing applications, the overall linearity of an ADC is usually expressed in the form of signal/(noise + distortion). This parameter is determined by applying a full scale low distortion sine wave into the converter and using the DFT (Discrete Fourier Transform) to determine the spectral density characteristics of the converter. The signal/noise and signal/(noise + distortion) ratios can then be computed from the spectral density data.



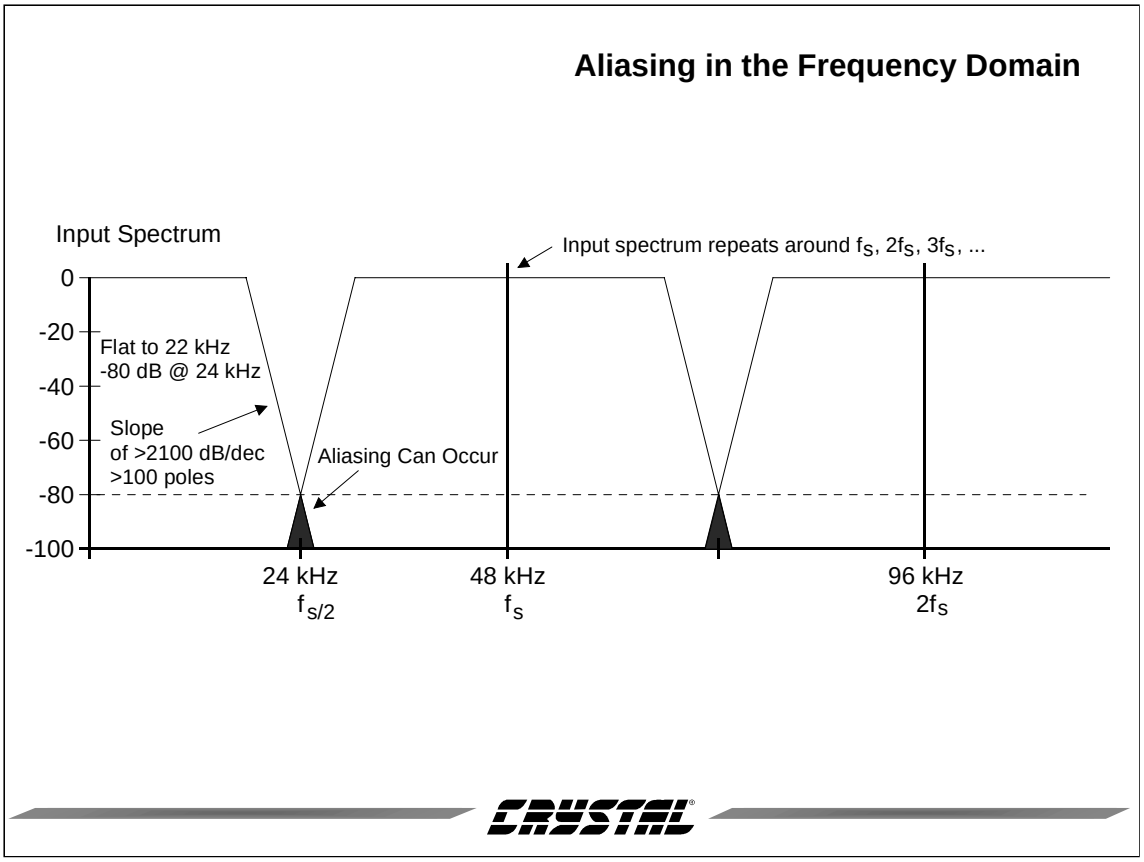
Offset error is a shift in the zero point of the transfer function.



Gain error is a change in the slope of the converter's transfer function relative to the stated reference voltage.



Sampling a signal at less than twice its maximum frequency causes aliasing, also known as folding. Those frequencies which are greater than half the sampling rate appear as frequencies which are less than half the sampling rate. The time domain drawing shows the mechanism by which this occurs.



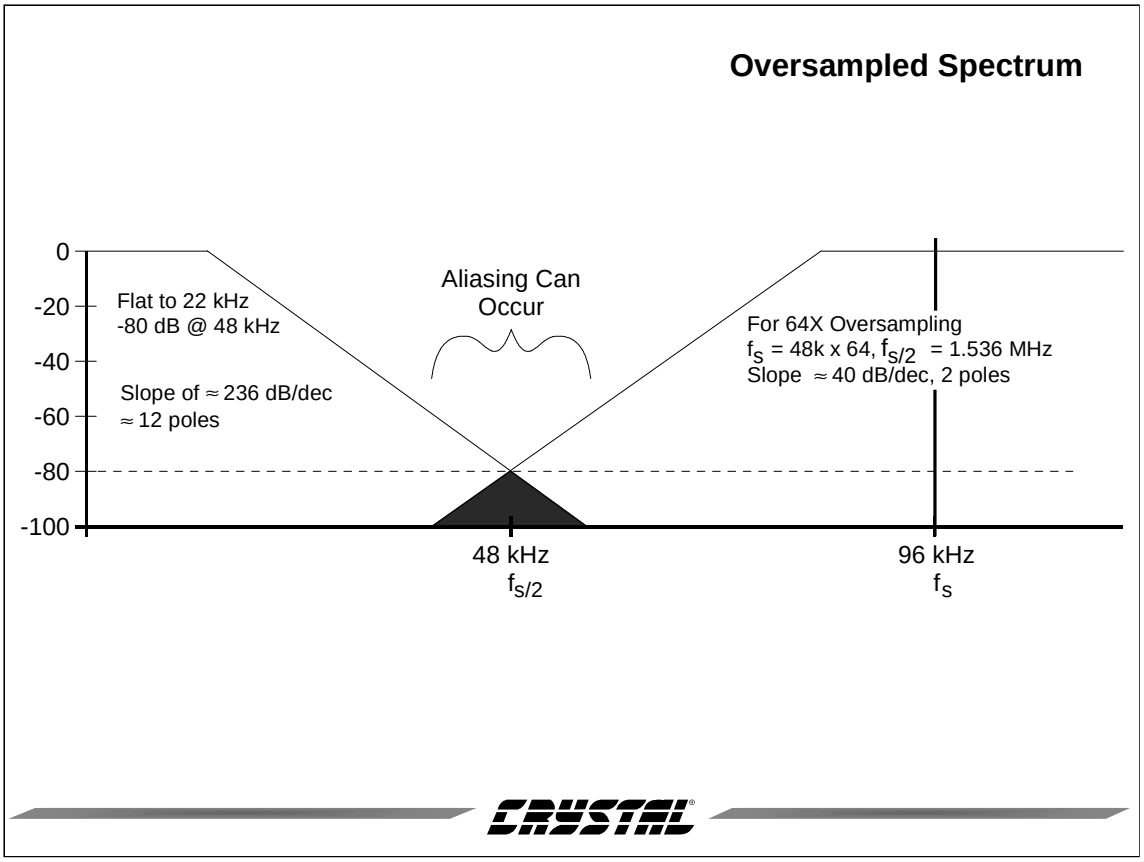
Here is the same effect shown in the frequency domain. Sampling a signal causes a copy of the input spectrum to appear around the sampling frequency. The copy hits the original input spectrum at $f_s/2$, and any significant amplitude components will be noticeable above the noise floor.

This can actually be used to frequency shift a high frequency signal to a lower frequency band. Typically though, the design engineer wants to avoid aliasing, since the folded high frequency information corrupts the wanted in-band signal.

This slide illustrates a converter sampling at 48 kHz, a typical sample rate used in digital audio. To achieve proper spectral measurement, the input signal should be limited to frequencies to less than 24 kHz. Preventing spectral components above 1/2 the sample rate can be difficult. In this illustration, the system application desires an audio bandwidth out to 22 kHz, but must prevent aliasing of frequencies above 24 kHz.

To achieve a 22 kHz bandwidth with 80 dB attenuation of frequencies at 24 kHz or greater requires a filter with a transition band only 2 kHz wide and a slope greater than 2100 dB/decade. A filter this complex would exceed 100 poles. This is impractical to achieve with an analog anti-alias filter. Most commercially-available analog anti-alias filters use at least an octave bandwidth to reach maximum cut-off; and then only achieve 60 dB typical attenuation. They generally utilize elliptical filter topologies and exhibit ripple in the passband and in the cut-off region of the filter.

Because of the limitations of analog filters, it can be beneficial to sample at greater than twice the signal bandwidth.



If the sample rate for a given bandwidth is increased, the complexity of the anti-alias filter can be reduced. In our previous audio example, the signal bandwidth was 22 kHz with a sample rate of 48 kHz. If the sample rate is doubled to 96 kHz, the anti-alias filter has more frequency bandwidth to reach 80 dB attenuation. The 100 pole filter requirement of the 48 kHz sample rate example is now reduced to only 12 poles.

Oversampling reduces the complexity of the anti-alias filter. This is one of the key benefits of oversampling. It is common for Analog-to-Digital Converters which use oversampling as part of their architecture to oversample by ratios of 64X, 128X, and even as high as 512X. With 64X oversampling, the filter requirement of our audio example is reduced to a two pole filter.

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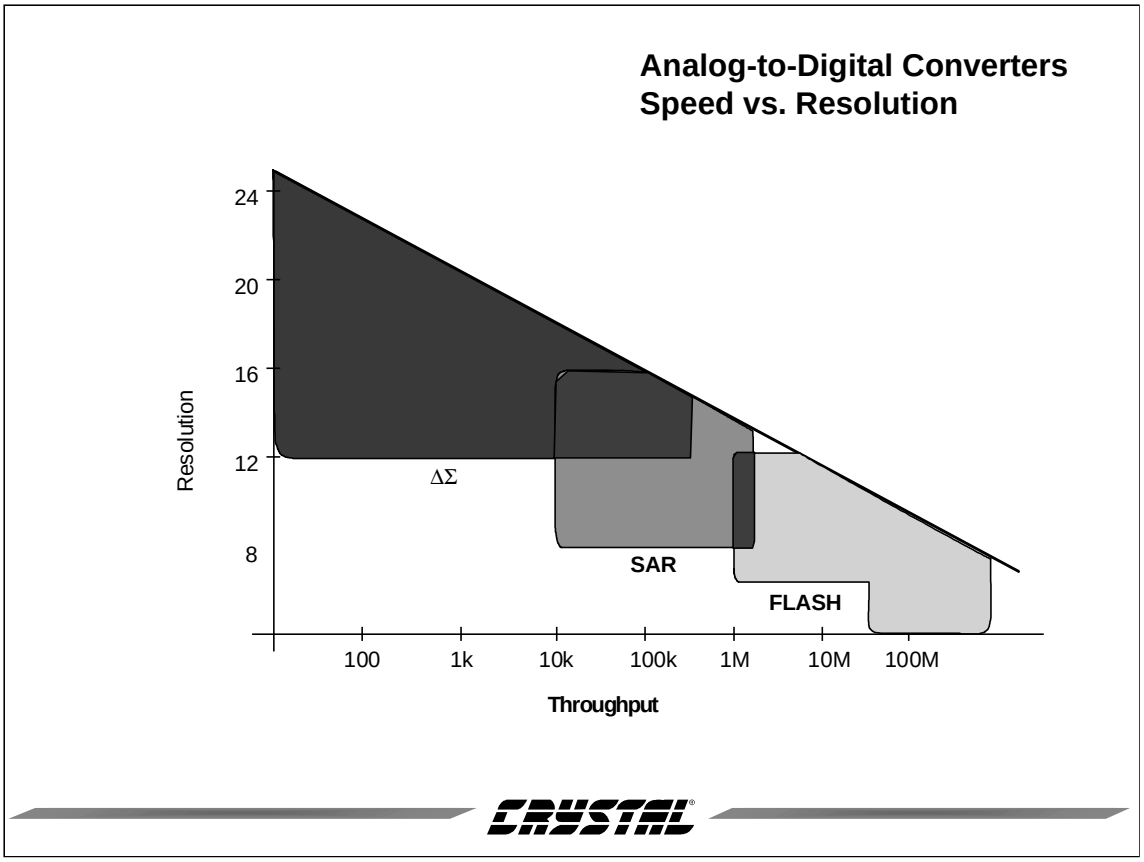
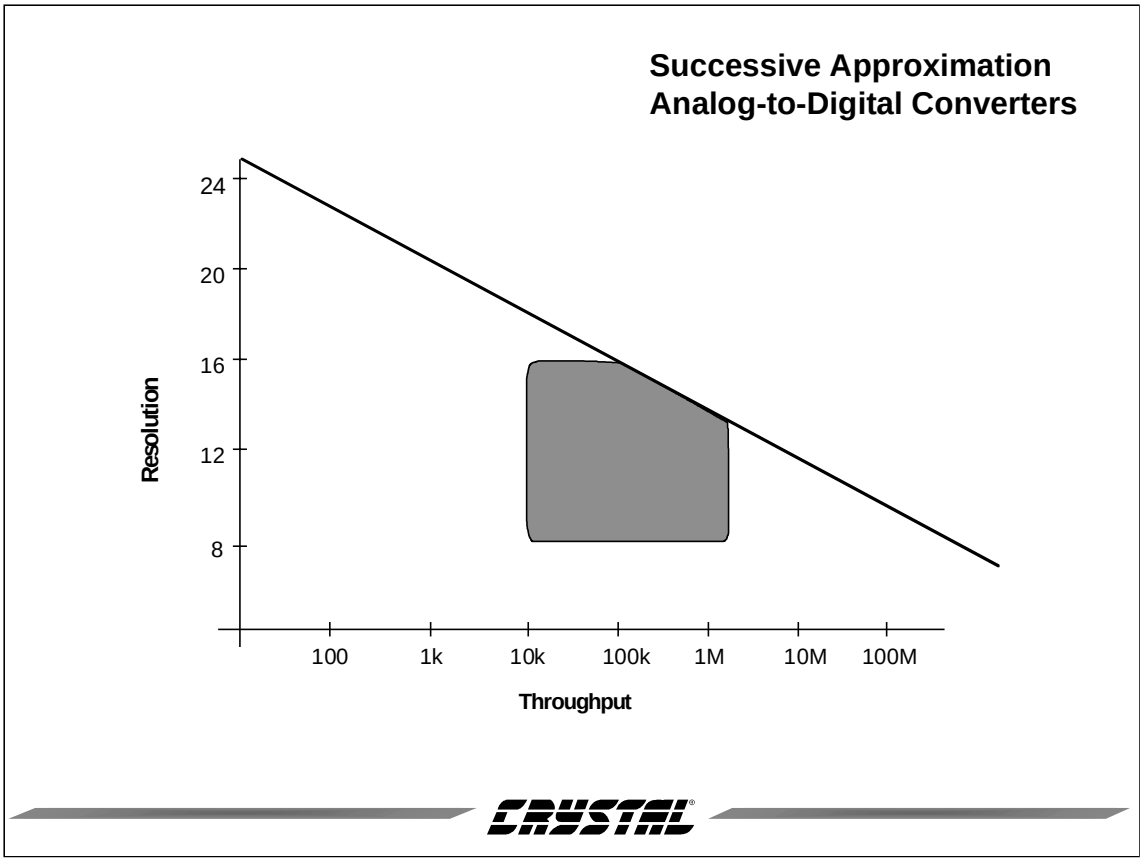


There are many Analog-to-Digital converter architectures; each having its particular benefits. This chart illustrates typical resolution and throughput of the Flash, Successive Approximation and ΔΣ converter architectures.

The Flash converter serves to digitize the higher frequencies, although it does so with less resolution.

Successive Approximation converters serve the intermediate range of frequencies, often being used in multiplexed applications to digitize many channels of lower frequency information.

ΔΣ converters are oversampling converters and perform well at effective sampling frequencies below 200 kHz bandwidth.



Successive approximation register (SAR) Analog-to-Digital Converters (ADCs) are available with a wide variety of performance attributes. Some are optimized for speed while others are optimized for low power. For this reason, SARs range in speeds from the low kilohertz range to the megahertz range. While 12-bit SARs are most common, 16-bit SARs are becoming the norm for new designs.

The Successive Approximation Analog-to-Digital Converter

In the successive approximation architecture, the analog input is successively compared to the output of a Digital-to-Analog Converter (DAC) controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (Most Significant Bit (MSB) on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters full scale. This procedure continues until all bits have been exercised.

Most of today's Successive Approximation Analog-to-Digital Converters use binary-weighted capacitive arrays. An advantage of capacitive-based construction is the inherent sample/hold function of the capacitor array.

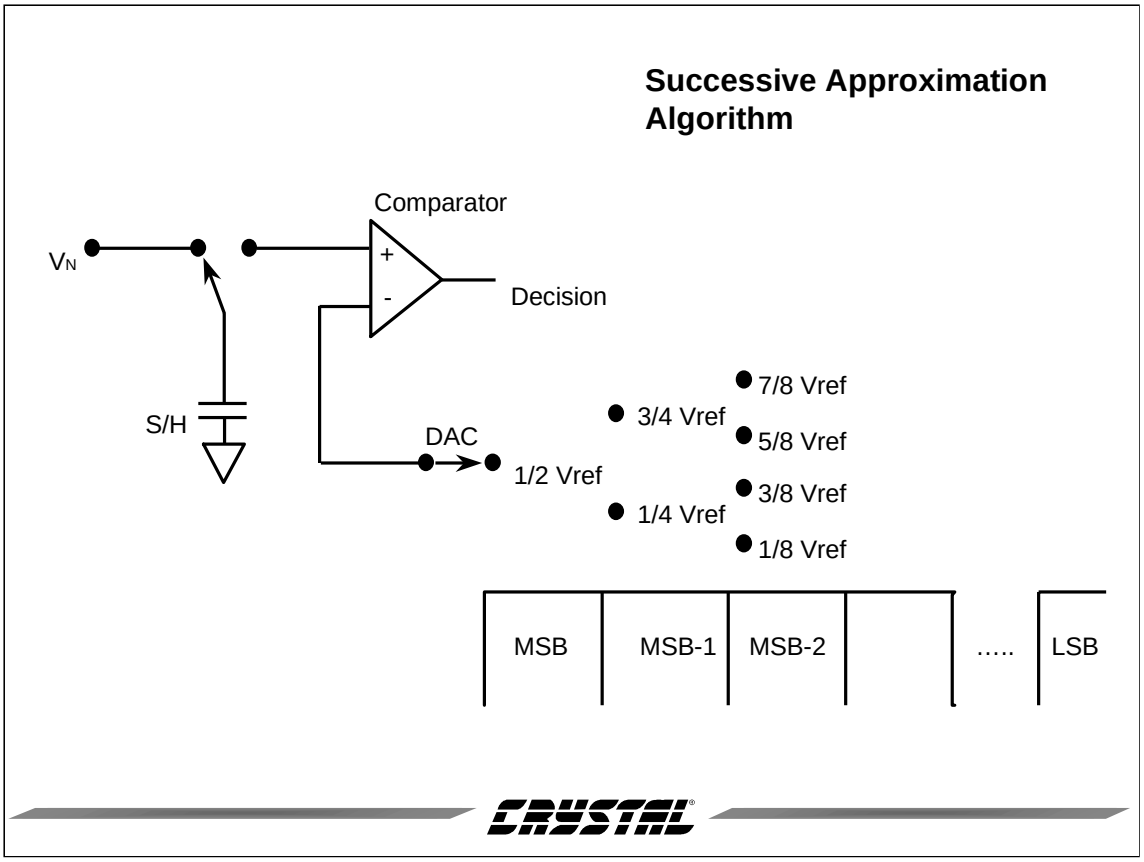
Crystal offered the first 16-bit self-calibrated capacitive-based Successive Approximation Analog-to-Digital Converter (SAR) in 1986. The Cirrus Logic Crystal CS5016, and its derivatives, still offer the highest performance available.

In the capacitive-based SAR, all the capacitors share a common node at the comparator's input. Their other terminals are capable of being connected to the analog input, the voltage reference, or to ground. In the capacitive-based converter, the conversion process consists of manipulating the free plates of the capacitor array to the voltage reference or ground. The first step of the successive approximation algorithm is to tie the MSB capacitor to the voltage reference and all other capacitors to ground. This forms a voltage divider whose center node is the input to the comparator. The comparator makes a decision as to whether the input voltage captured on the capacitor array is greater or less than half scale. Continuing the successive approximation algorithm involves manipulating the capacitor connections to go through the various capacitor divider ratios, testing the resultant voltage with the comparator.

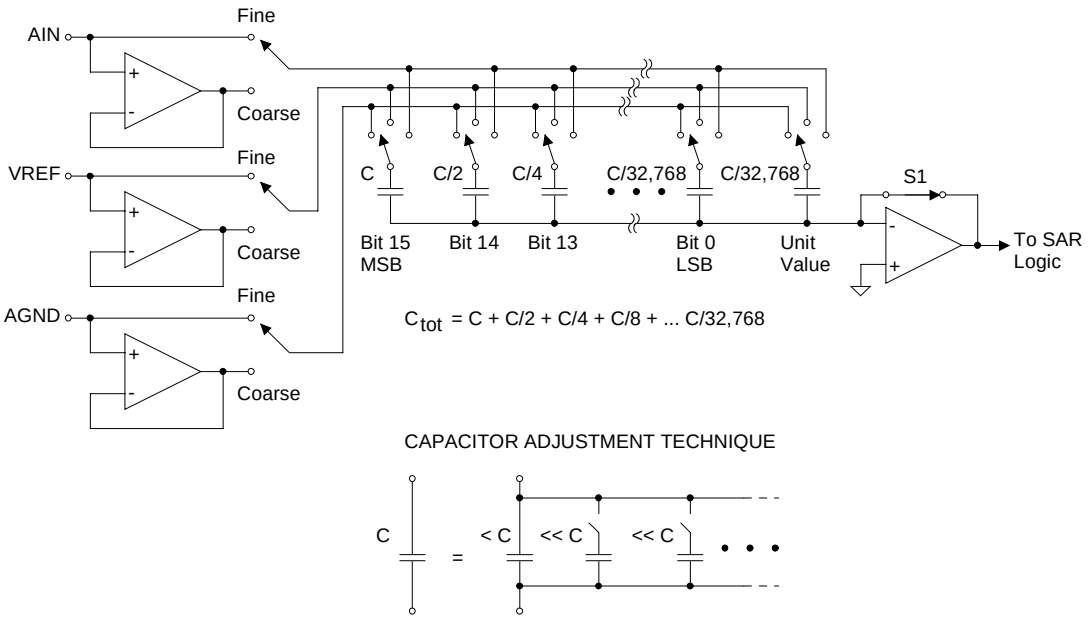
The SAR converter has a multi-point transfer function in which the accuracy is largely determined by the accuracy of the elements which make up the DAC. Ratio errors in the sizes of the Digital-to-Analog elements cause Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) errors; and can even result in missing codes.

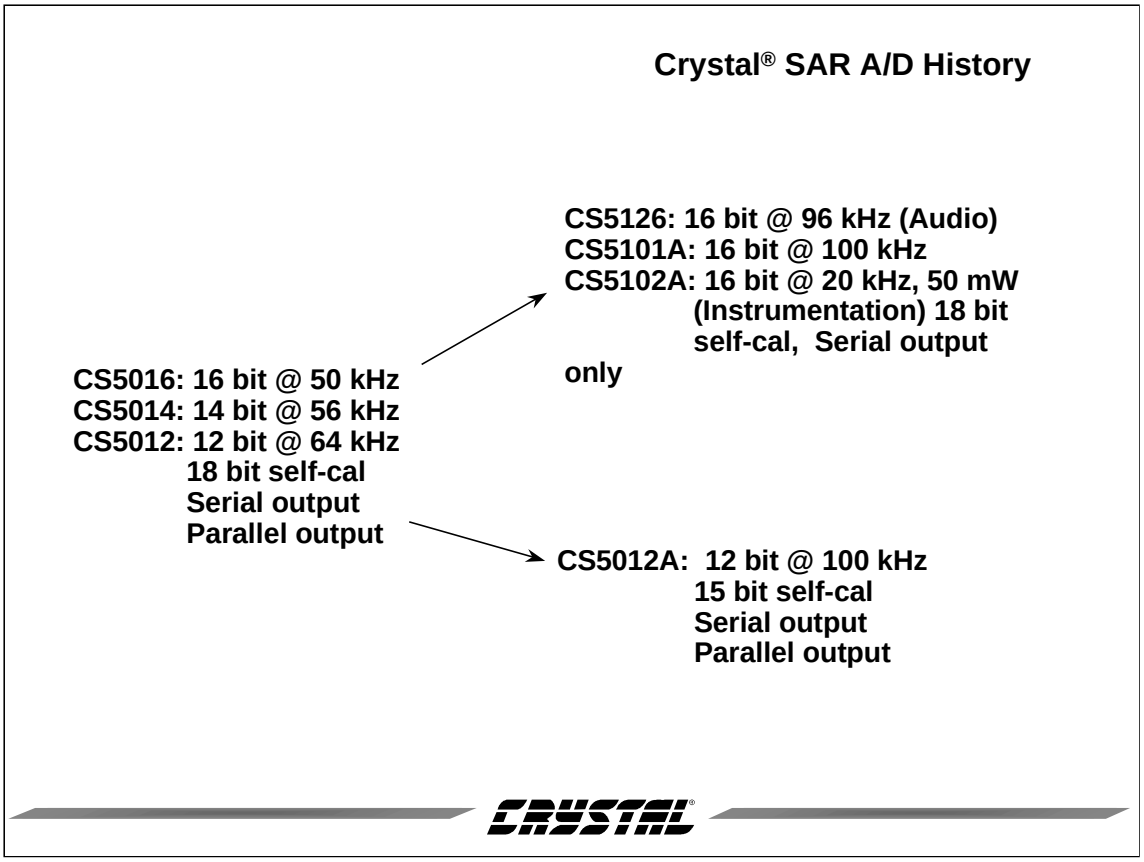
The self-calibration technique used in Crystal SARs calibrates the size of each array capacitor by switching small adjustment capacitors in parallel across each main capacitor. Each capacitor in the array is adjusted to 18-bit resolution. This results in superior INL and DNL performance. The "all-capacitor" approach results in capacitor tempco tracking near 0.2 ppm/C.

Non-Crystal capacitive-array SARs typically use R-2R D/A converters to inject a correction voltage into the summing node of the capacitor array to correct for capacitor weighting errors.


Successive Approximation Algorithm
Comparator
VN
+
-
Decision
S/H
DAC
1/2 Vref
3/4 Vref
1/4 Vref
7/8 Vref
5/8 Vref
3/8 Vref
1/8 Vref
MSB
MSB-1
MSB-2
.....
LSB

Successive Approximation Analog-to-Digital Converter Charge Balancing Architecture



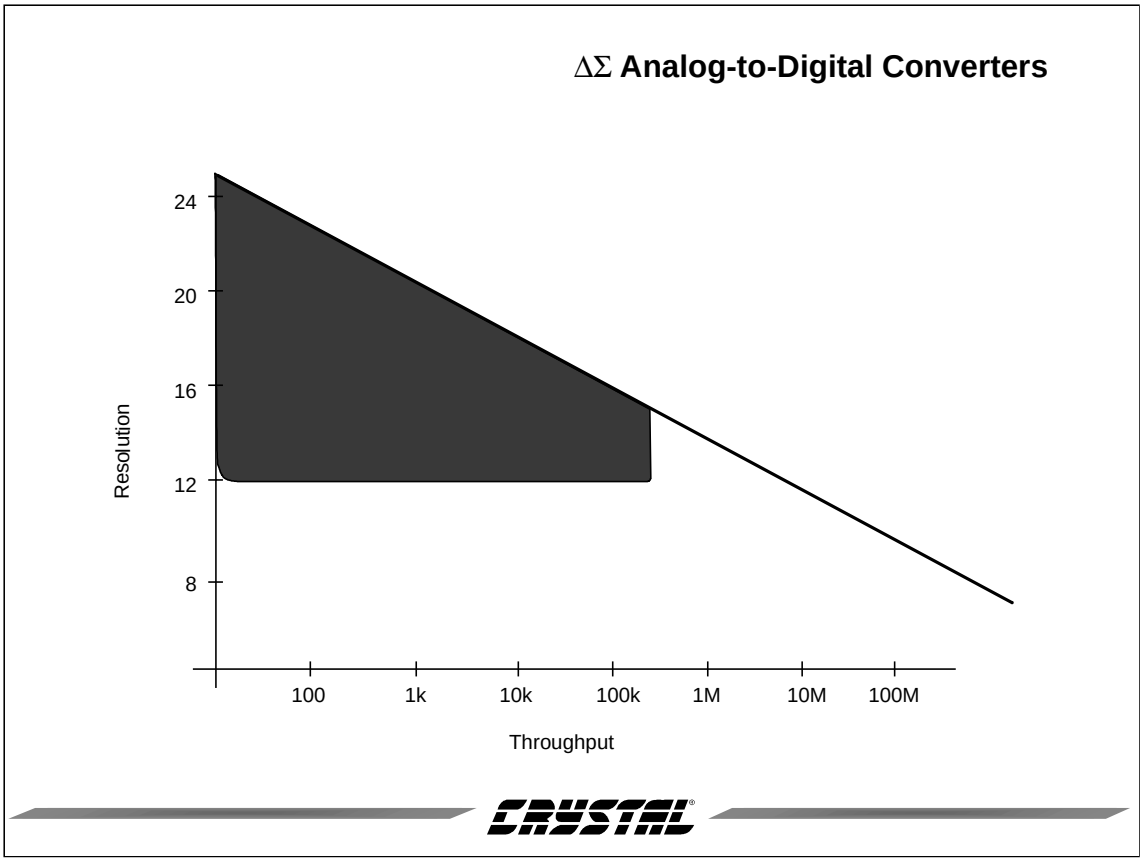


The CS5016 was the first SAR converter designed at Cirrus Logic. The device includes a calibration engine which calibrates the capacitor ratios in the SAR feedback DAC to 18-bit resolution. This yields DNL of 1/4 LSB at 16 bits. The CS5016 was short-cycled to yield the CS5014 and the CS5012. It takes two fewer clock cycles for the successive approximation algorithm to finish in the CS5014 than in the CS5016; and four fewer clocks in the CS5012; therefore have higher conversion speeds.

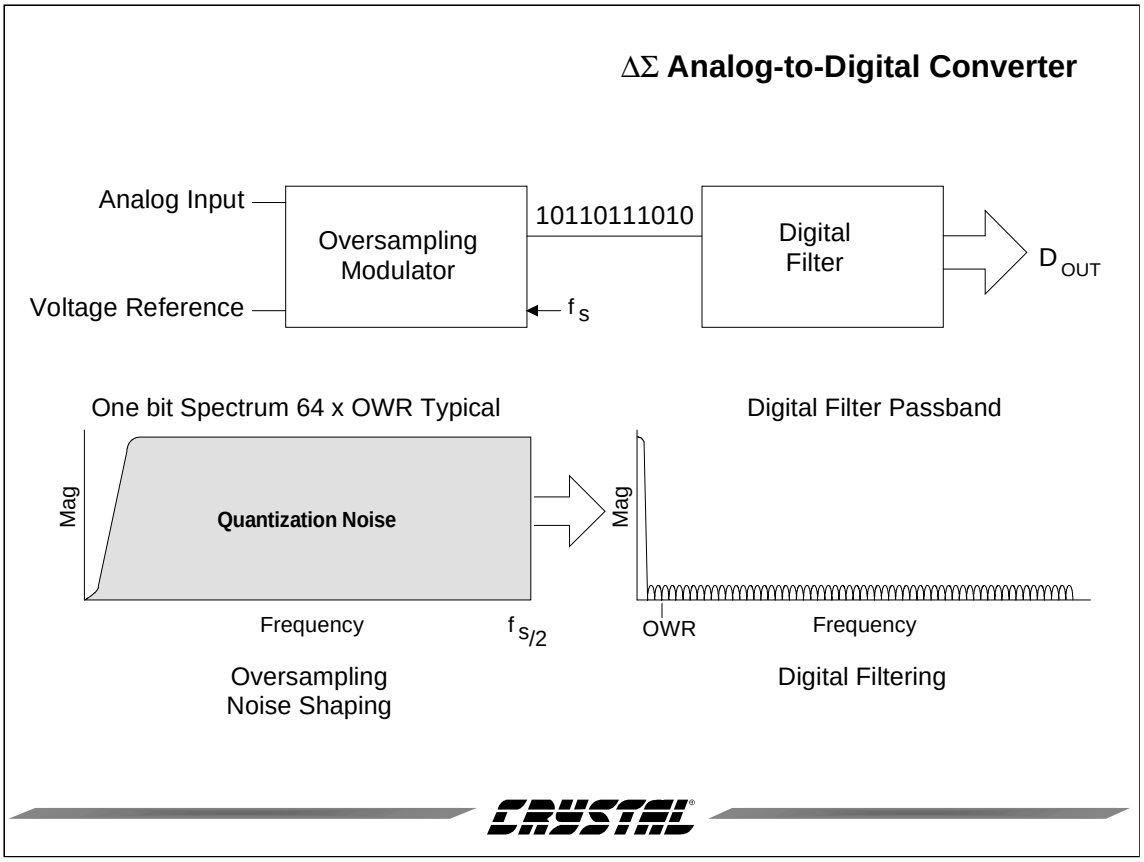
The CS5126 was originally designed as the first stereo audio converter offered by the company (before the introduction of delta-sigma converters). It runs from a master clock of 24.576 MHz (common in audio) to yield a 96 kHz stereo output. The CS5101A is an industrial version which is designed to run over higher temperatures. The CS5102A is a low power version of the CS5101A; and is the most accurate low-powered SAR in the marketplace. Each of these parts, the CS5101A and CS5102A, includes an 18-bit self-calibration engine.

The CS5012A is a CS5012 are modified to use a 15-bit self-calibration engine. This still results in the most accurate 12-bit ADC on the market and also allows the capacitor array in the device to be smaller which results in a faster conversion rate.

This family of SAR converters are the most accurate in the world. See the FFT and DNL plots in the CS5101A/CS5102A data sheet. These plots illustrate the parts calibrated and operating at 25 C. Then the temperature is raised to 138 C without recalibration. Only a minor change in performance occurs. Note that the CS5016 and CS5101A has a full scale drift of only a few codes over -55 to +125 C. This is 20-50 times better than competitors parts over even less temperature change.



ΔΣ Analog-to-Digital Converters are used in a broad range of applications, from dc to over 500 kHz. At lower frequencies, the ΔΣ architecture can yield much higher converter resolution.

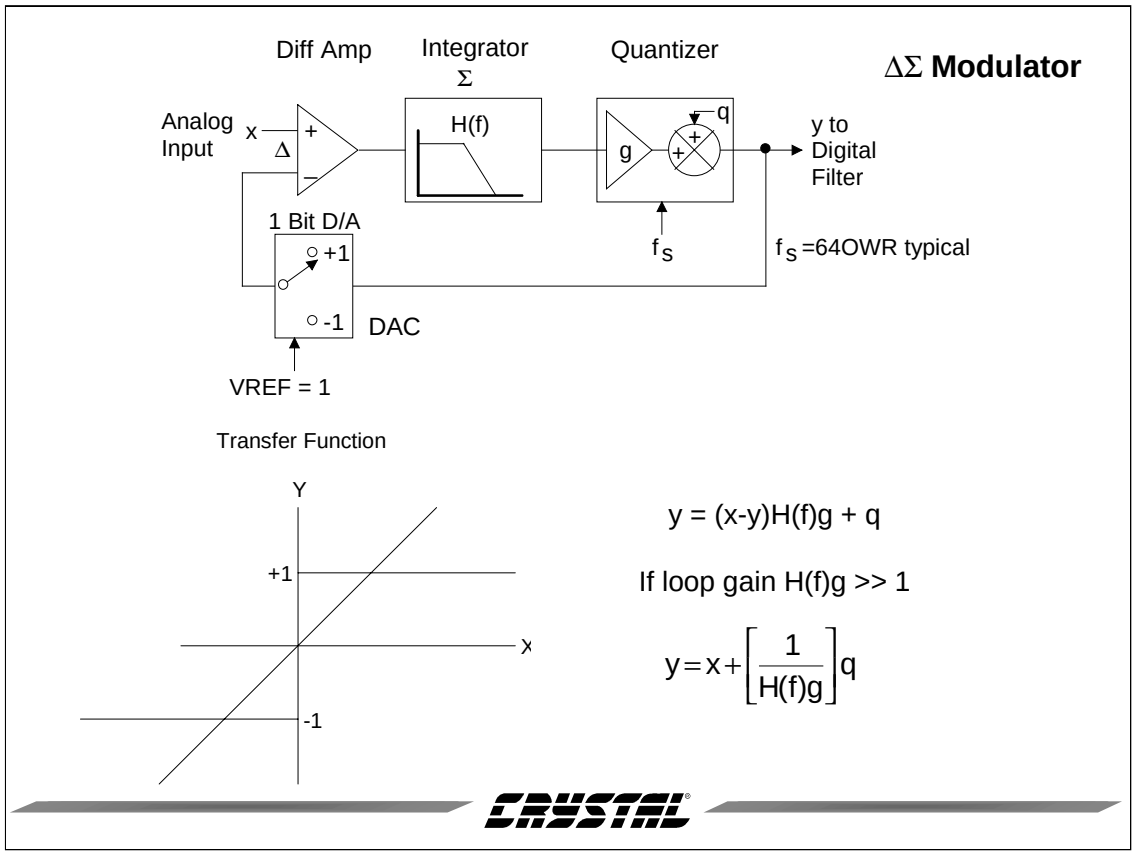


The ΔΣ converter uses oversampling as a fundamental means of achieving high resolution. The converter includes an oversampling modulator followed by a uniquely designed digital filter. The modulator is usually composed of a 1-bit sampler running at very high sample frequencies relative to the signal being digitized. Oversampling ratios of 64, 128, and 256 are common.

But oversampling alone is not enough. The 1-bit sampler has very high quantization error, and consequently, very high quantization noise, relative to the input signal. To achieve high signal to noise, the oversampling modulator includes a noise-shaping filter which suppresses the quantization noise over the input signal bandwidth. This results in a digital bit stream out of the modulator which is spectrally filtered.

The bit stream is then processed by a digital filter which is designed to take advantage of this noise-shaped spectrum. The digital filter processes the 1-bit samples, removing the "out-of-band" quantization noise while at the same time increasing the converter resolution.

ΔΣ Analog-to-Digital converters use oversampling, noise shaping, and digital filtering together to yield a low speed, high resolution output from a high speed low resolution sampler.



The ΔΣ modulator consists of a differential amplifier which measures the delta difference between the input signal and a 1-bit feedback Digital-to-Analog converter. The Δ (delta) is amplified and applied as the input to a filter which consists of several integrator stages. The integrators "sum up" the error voltage, hence the name Σ (sigma) for the filter block. The greater the number of integrators in the noise-shaping filter, the better the quantization noise can be suppressed within the bandwidth of interest.

Each additional integrator adds 6 dB of signal/noise improvement for a doubling of the sample rate. This happens because each additional integrator increases the filter roll-off by 6 dB per octave increase of frequency. The number of integrators in the noise-shaping filter indicates the modulator order of a ΔΣ converter.

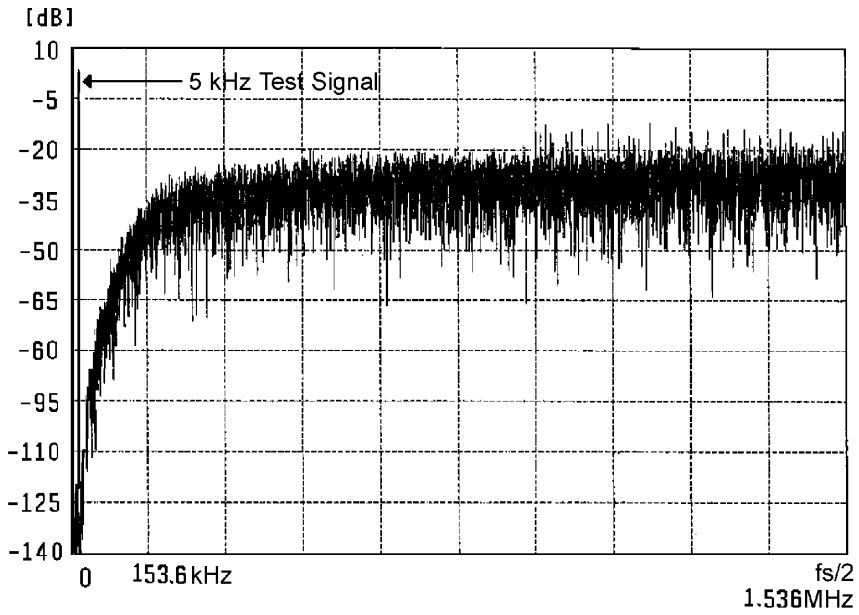
The output of the noise-shaping filter is then quantized. Use of a single comparator as the quantizer of a ΔΣ Analog-to-Digital converter is common because a comparator is a "one bit" converter. A 1-bit converter requires no matched components. This results in a two point transfer function which is inherently linear.

The output of the comparator results in a bit stream with a 1s density proportional to the ratio of the input signal and the reference voltage of the feedback Digital-to-Analog Converter. Realize that the Digital-to-Analog converter is in a feedback loop where its output is trying to minimize the error voltage at the inputs of the differential amplifier.

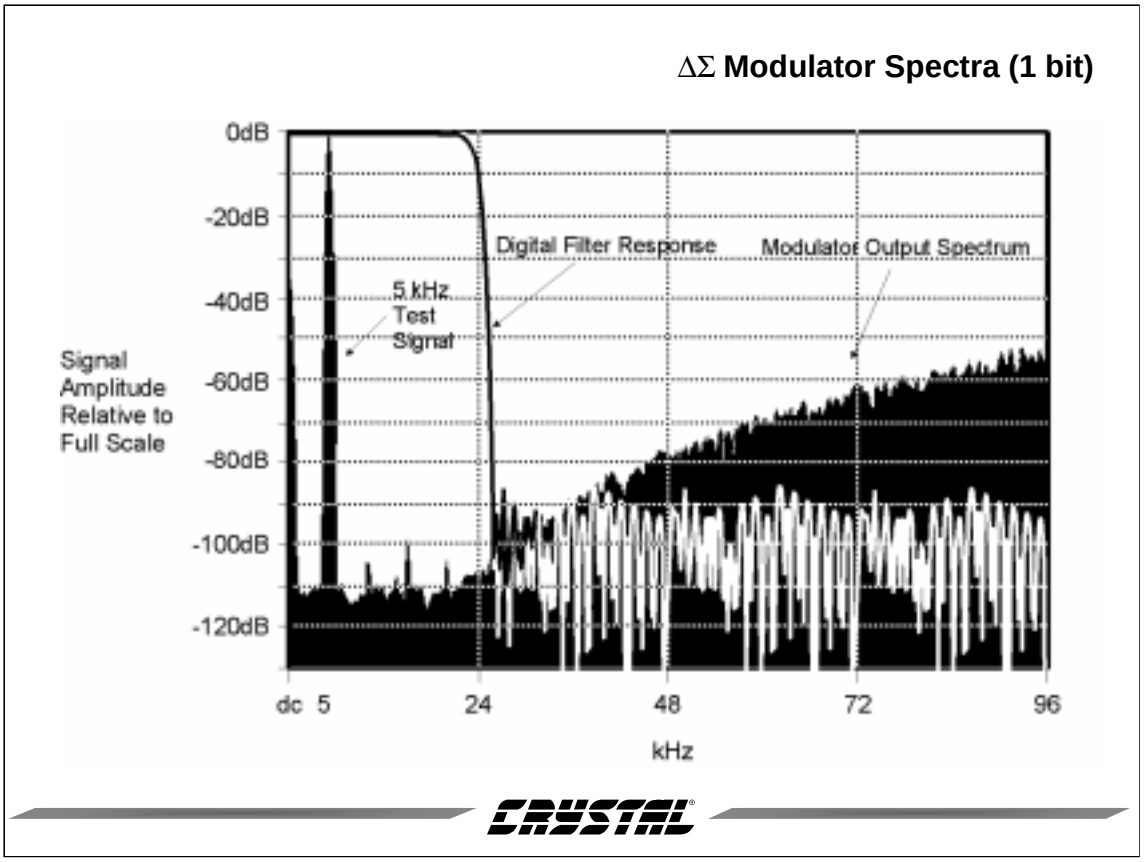
As the input signal goes positive, the differential amplifier error voltage will cause the Digital-to-Analog converter to spend more clock periods putting out +1. For this to occur more 1s will need to be generated by the comparator. As the signal goes negative, just the opposite is true. Hence, the 1s density out of the modulator will be proportional to the input signal.

The modulator gain equation indicates how the noise-shaping filter reduces the quantization noise.

ΔΣ Modulator Spectra (1 bit)

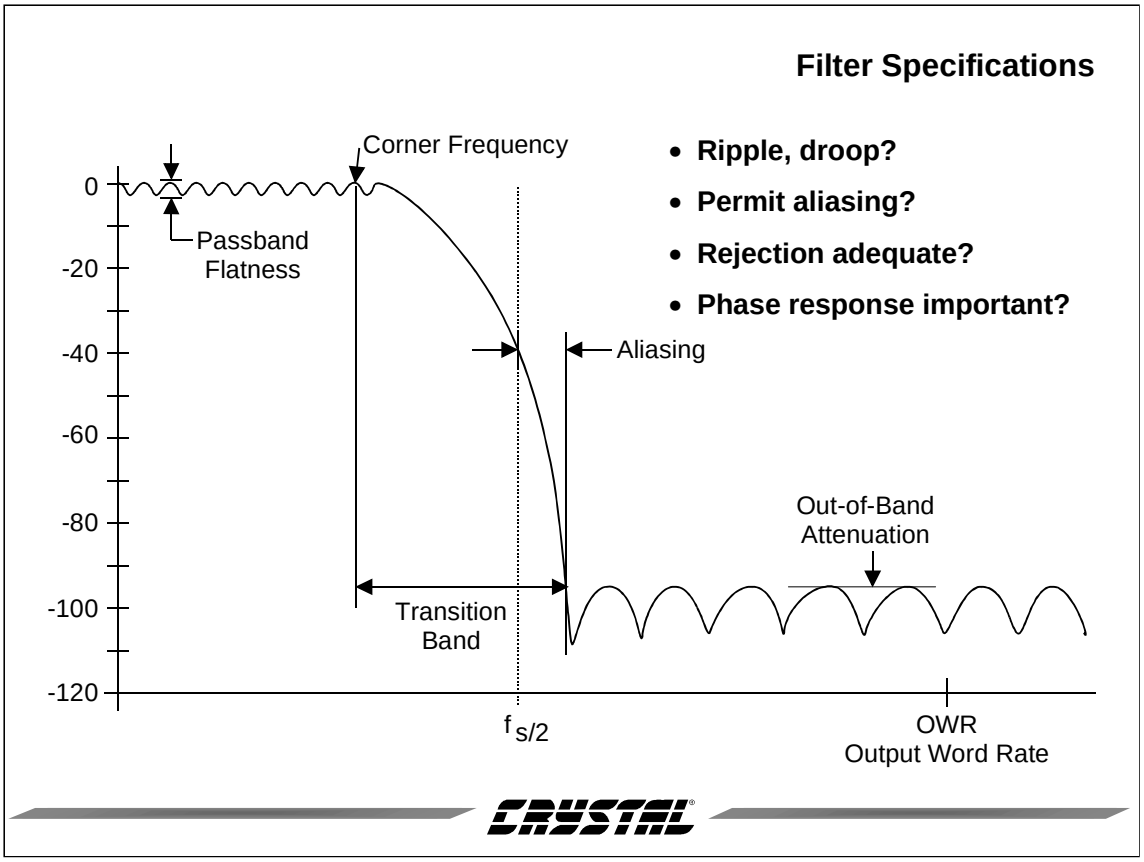


This slide illustrates the spectrum of the modulator 1-bit output bit stream. Notice that the noise-shaping filter suppresses the quantization noise only over a very small portion of the dc to f_s / 2 bandwidth. If the signal/noise ratio for this modulator spectrum was computed for the Nyquist bandwidth (dc to 1.536 MHz), the result would be that of a 1-bit Analog-to-Digital converter.



The noise-shaped bit stream is then processed by the digital filter. The digital filter is designed in conjunction with the noise shaping of the modulator to result in the desired signal/noise ratio across the digital filter bandwidth. The filter rejects the out-of-band quantization noise.

The digital filter determines much of the behavior of the ΔΣ Analog-to-Digital converter. The modulator is oversampling at much higher frequencies than the signals of interest, therefore it is designed to operate with minimal effects on the signal being processed.



In a ΔΣ Analog-to-Digital converter, the digital filter dominates the signal behavior of the device. The digital filter will determine:

a) the signal bandwidth

b) the flatness of the passband

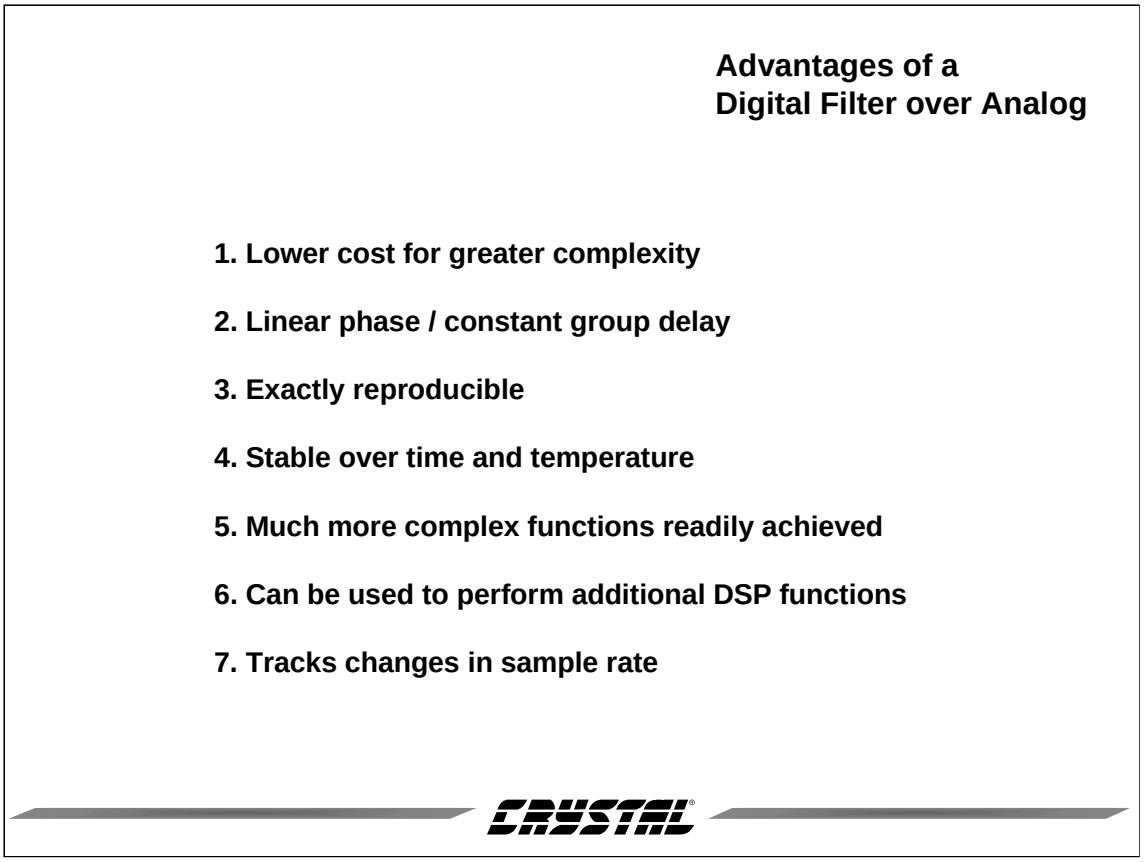
c) the phase response over the passband

d) the group delay

e) the transition band characteristics

f) the out-of-band attenuation

The digital filter can also be designed to prevent aliasing. In applications with transient inputs, the filter will dictate the settling time characteristics.



Digital filtering offers a number of advantages over analog filtering.

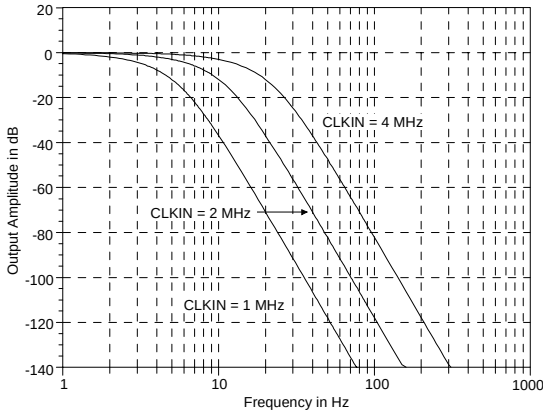
They offer more complex filtering functions at much lower cost. Many of the digital filters found in Cirrus Logic Crystal delta-sigma devices achieve 1000s of taps of filtering. An analog filter would require a similar number of poles and zeros if it were to achieve comparable performance. An analog filter of this complexity is not realizable.

Digital filters offer linear phase performance which gives constant group delay, a highly desirable feature for audio applications.

A high level of integration supports multiple devices with exactly the same filter characteristics, which remain constant with time and temperature.

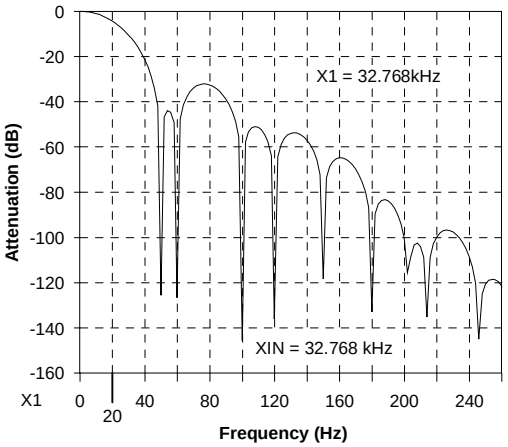
Digital Filter Comparison

CS5501/CS5503



-3 dB @ 10 Hz (Clock = 4 MHz)
Output Word Rate = 4 kHz
Settling time ≈ 130 ms.

CS5504 Family



-3 dB @ 17 Hz (Clock = 32.768 kHz)
Output Word Rate = 20 Hz
Settling Time = 50 ms

It is helpful to examine the characteristics of some digital filter functions found in various delta-sigma converters.

Understanding that the digital filter in a delta-sigma converter defines the frequency characteristics of the device will help the analysis of how these characteristics affect a specific application.

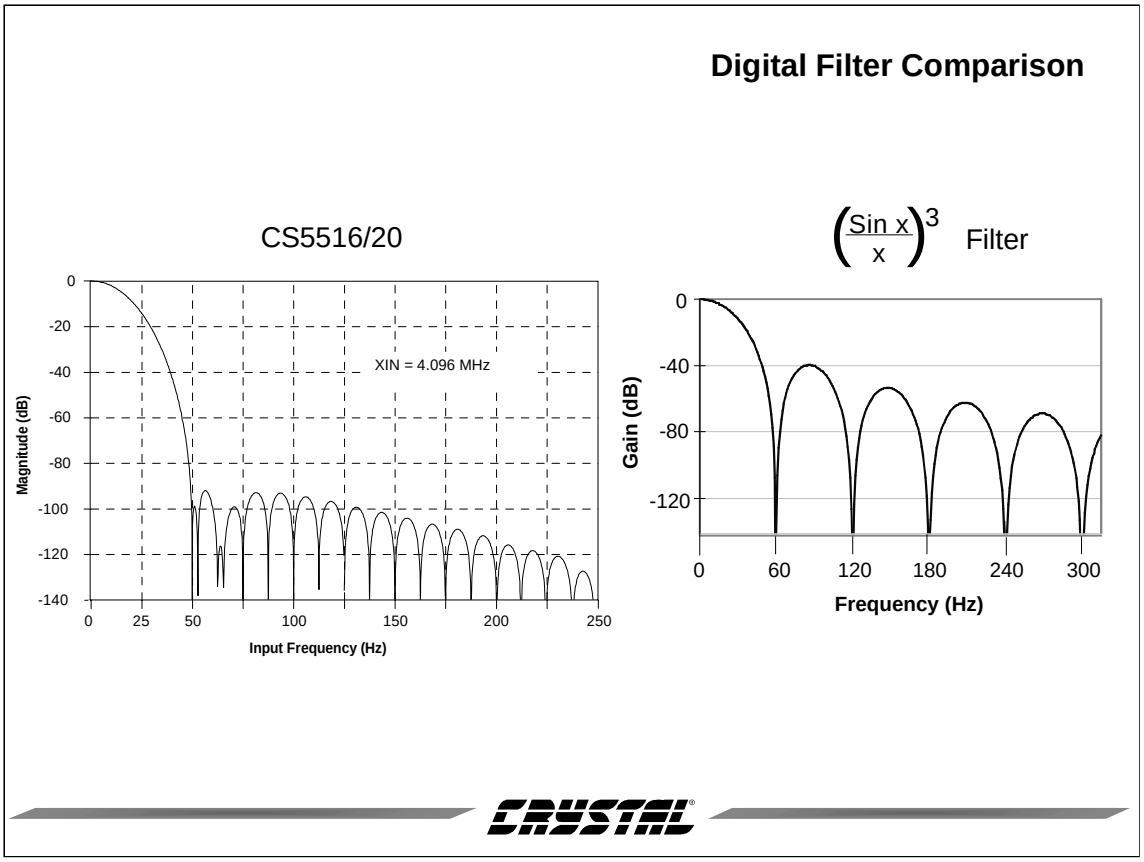
The Cirrus Logic Crystal CS5501/CS5503 filter, shown above, is a 6 pole Gaussian filter with a -3 dB bandwidth of 10 Hz (CLKIN = 4 MHz). The filter rolls off at approximately 36 dB/octave above 10 Hz. It has very good out-of-band attenuation but the converter can not be multiplexed. The settling time for an input step is about 130 milliseconds. With multiplexed inputs, a throughput rate of about 7 samples per second can be achieved.

The CS5504 family of converters has a much faster settling time.

The plot above shows that the filter's Nyquist frequency is 10 Hz and this converter has an output word rate of 20 samples/second.

It is designed to settle to full accuracy in one conversion (50 msec. with XIN =32.768 kHz); consequently, the filter design has very low attenuation. In order to achieve the settling requirement, the filter allows aliasing.

The filter will also attenuate line harmonics of 50 and 60 Hz (and their multiples) when operated from a low cost watch crystal (32.768 kHz).

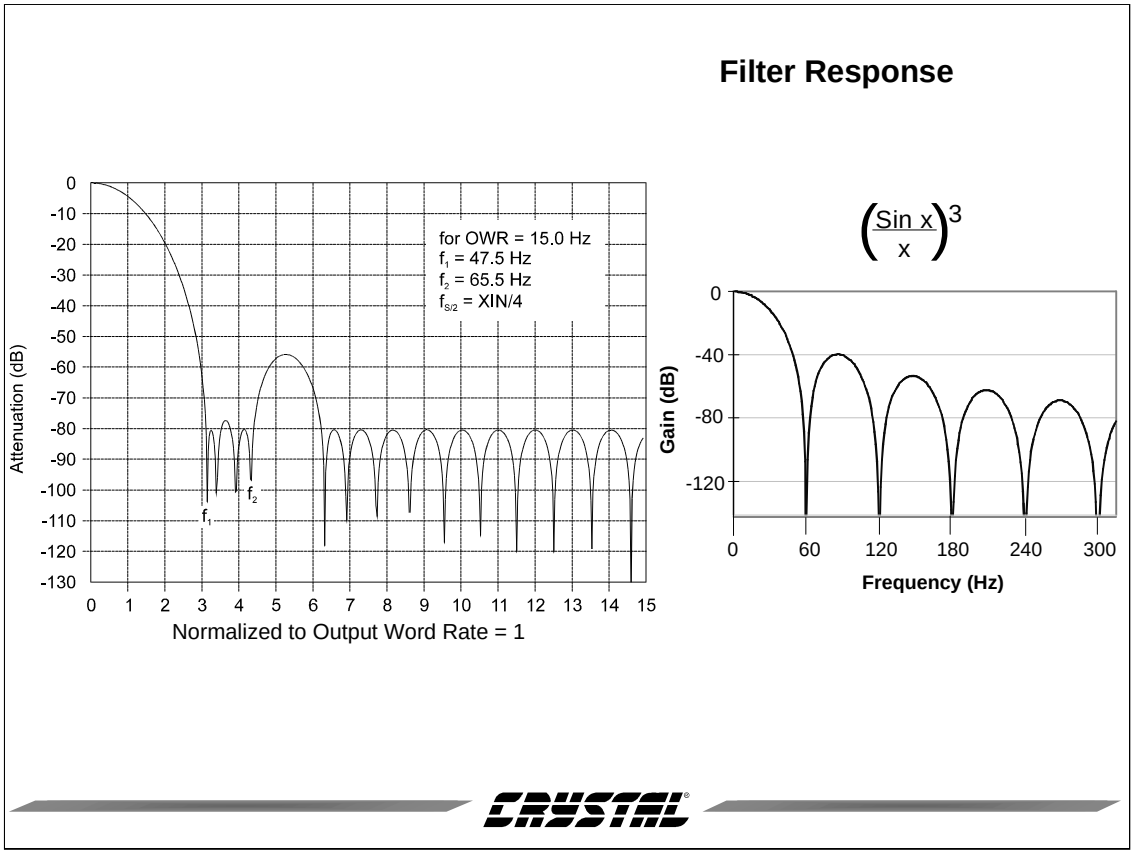


The Cirrus Logic Crystal CS5516/CS5520 is a delta-sigma converter which is optimized for static measurement of bridge transducers.

Its digital filter is designed to achieve good rejection of line frequencies and their harmonics. Rejection at frequencies above the line frequency is excellent with greater than 90 dB of out-of-band rejection.

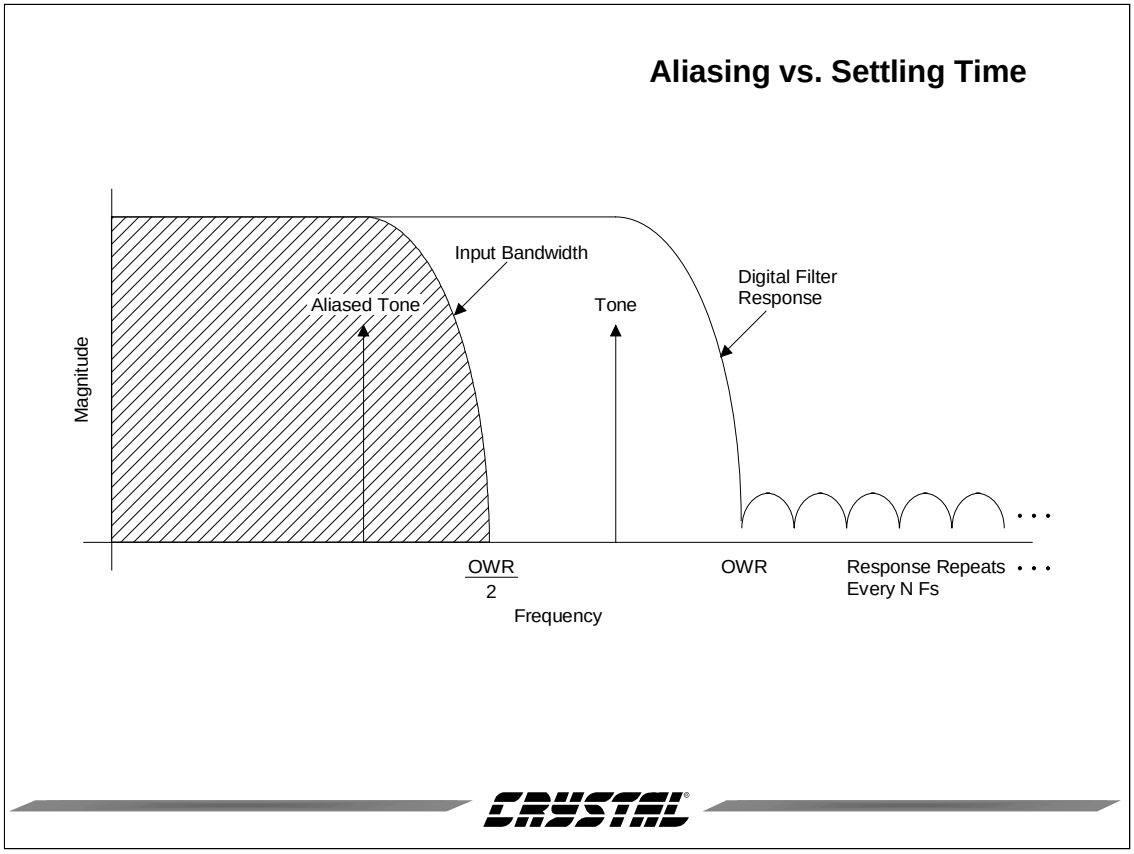
Note that if a crystal less than 4.096 MHz is used, that both 50 and 60 Hz are rejected with an attenuation which exceeds 90 dB.

A common filter found in non-Crystal products is the $(\text{Sinx/x})^3$ or Sinc^3 filter. This filter has greater notch width than the regular sinc filter, but the filter does not provide rejection for both line frequencies at the same time. The filter must be set-up for either 50 or 60 Hz rejection.



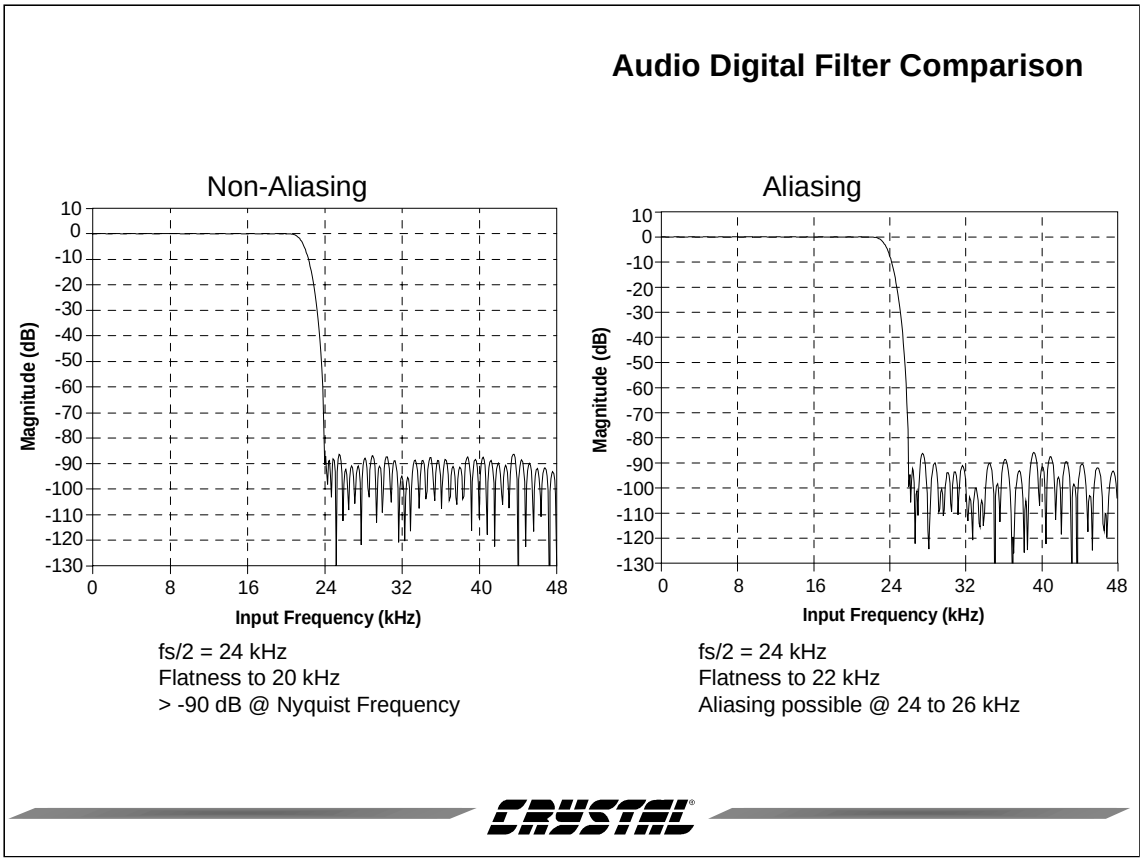
The CS552x family of converters has a filter response similar to the above plot. The filter's is designed to provide simultaneous 50 Hz and 60 Hz rejection and settle a full scale step input to full accuracy in one conversion cycle.

A Sinc3 filter, illustrated in the adjacent plot, is used in many DS ADCs. This filter rejects either 50 Hz or 60 Hz of rejection and must be reprogrammed to select between the two. The Sinc3 also takes 3 to 4 conversions to settle a full scale step input (full scale step input are likely to occur in multiplexed application).



As shown in the plot above, a tradeoff exists between a digital filter's ability to settle a full scale step to full accuracy in one conversion cycle and a digital filter's ability to eliminate aliasing.

Most dc measurement applications will not have frequencies that would produce aliasing components. Therefore, by relaxing the aliasing requirement, a digital filter can be designed to settle a full scale step input in one conversion. While using such a filter, the user should keep in mind that aliasing can and will occur if they are trying to digitize an input signal whose input frequency is from OWR/2 to OWR (Fs is the sampling rate and OWR is the output word rate of the ADC).



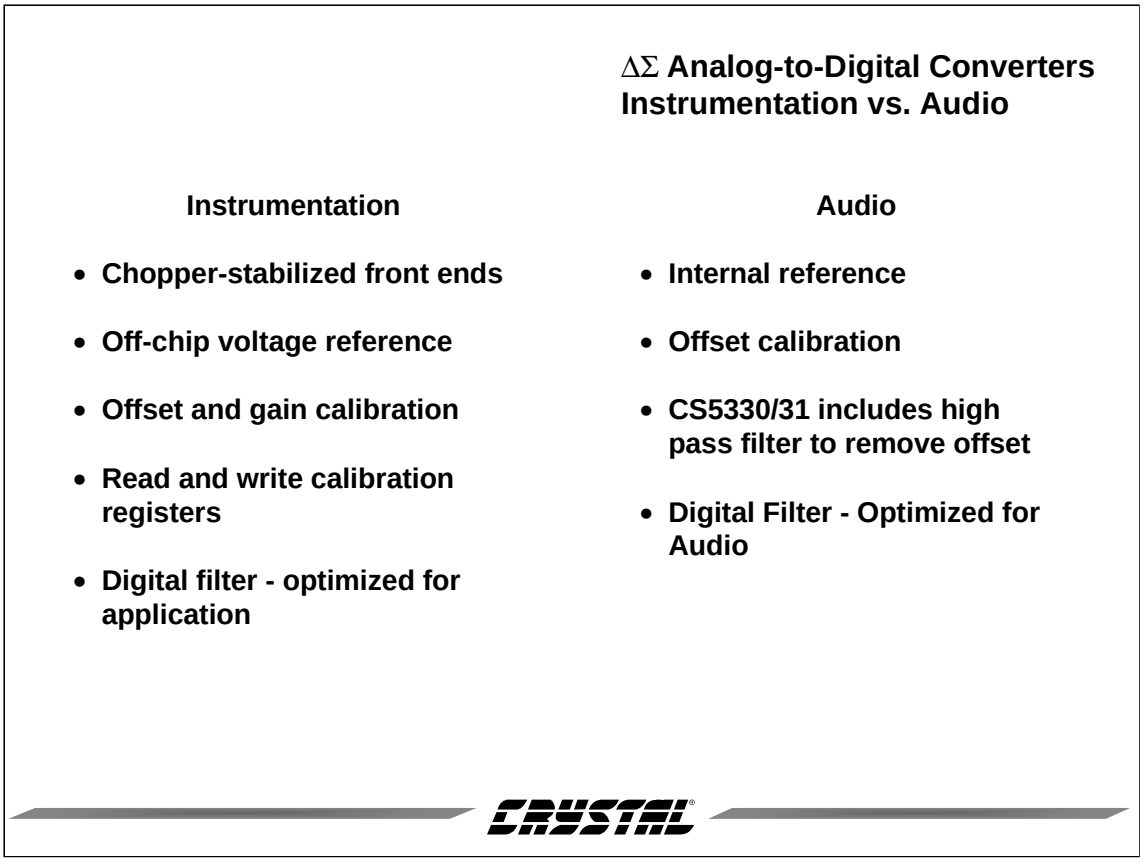
The plots above highlight the different preferences of various audio users.

The filter in the Analog-to-Digital Converter (ADC) on the left is designed to prevent aliasing. The filter is > -90 dB at the Nyquist frequency. This filter response is preferred in applications such as sonar and spectral measurement instrumentation (other than audio).

The filter in the ADC on the right is preferred for audio applications. The filter maximizes the passband over which the filter is flat (24 kHz versus 22 kHz for the previous filter). To achieve this wider passband, the filter allows aliasing of signals between 24 kHz and 26 kHz. This is acceptable in audio applications because the aliased components cannot be heard.

Aliasing filters are common in many different $\Delta\Sigma$ audio Analog-to-Digital converters. Allowing some aliasing reduces the filter complexity, reduces the number of filter taps and therefore lowers the product cost.

Fewer taps means less group delay through the filter. Minimized group delay is desirable in audio recording studio equipment where the signal may be processed through several Analog-to-Digital and Digital-to-Analog stages in the process of recording and mixing.



There are different requirements for Analog-to-Digital Converters (ADCs) designed for instrumentation and audio applications.

Instrumentation applications generally require accurate DC measurement capabilities which can be achieved with careful attention to the voltage reference stability and control of offsets. Instrumentation converters generally use an off-chip reference voltage which allows the system designer to fine tune the reference circuit to meet the system performance goals. The Cirrus Logic Crystal ΔΣ instrumentation converters also use chopper stabilized front ends to eliminate the effects of internally generated offset voltages.

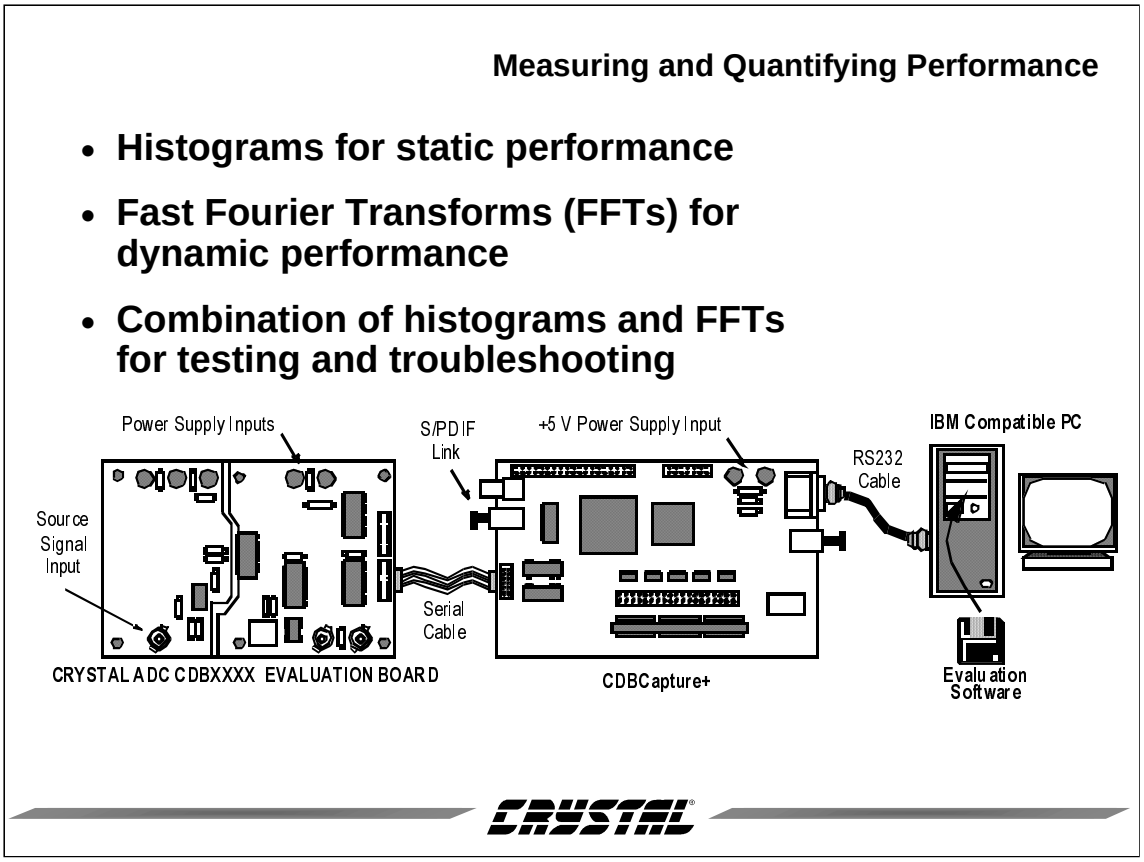
Audio applications are typically limited to a 20 Hz to 20 kHz bandwidth and are often more cost sensitive than instrumentation applications.

One approach to achieve the cost goal is to take advantage of the relaxed DC stability requirement. All Cirrus Logic Crystal audio ΔΣ converters include an on-chip voltage reference. They meet the requirements for audio applications but often will not meet the more stringent requirements for instrumentation.

Audio converters utilize several techniques to deal with offsets. All Crystal audio converters, with the exception of the CS5330/31, are capable of performing an offset calibration which will remove the measured offset at the time of calibration.

Applications Reference Guide - Section III

- Introduction to Analog-to-Digital Converters
- Analog-to-Digital Converter Topologies
- **Measurement, Testing and Troubleshooting**
- DAQ ADC Applications Examples
- Technical Support Services



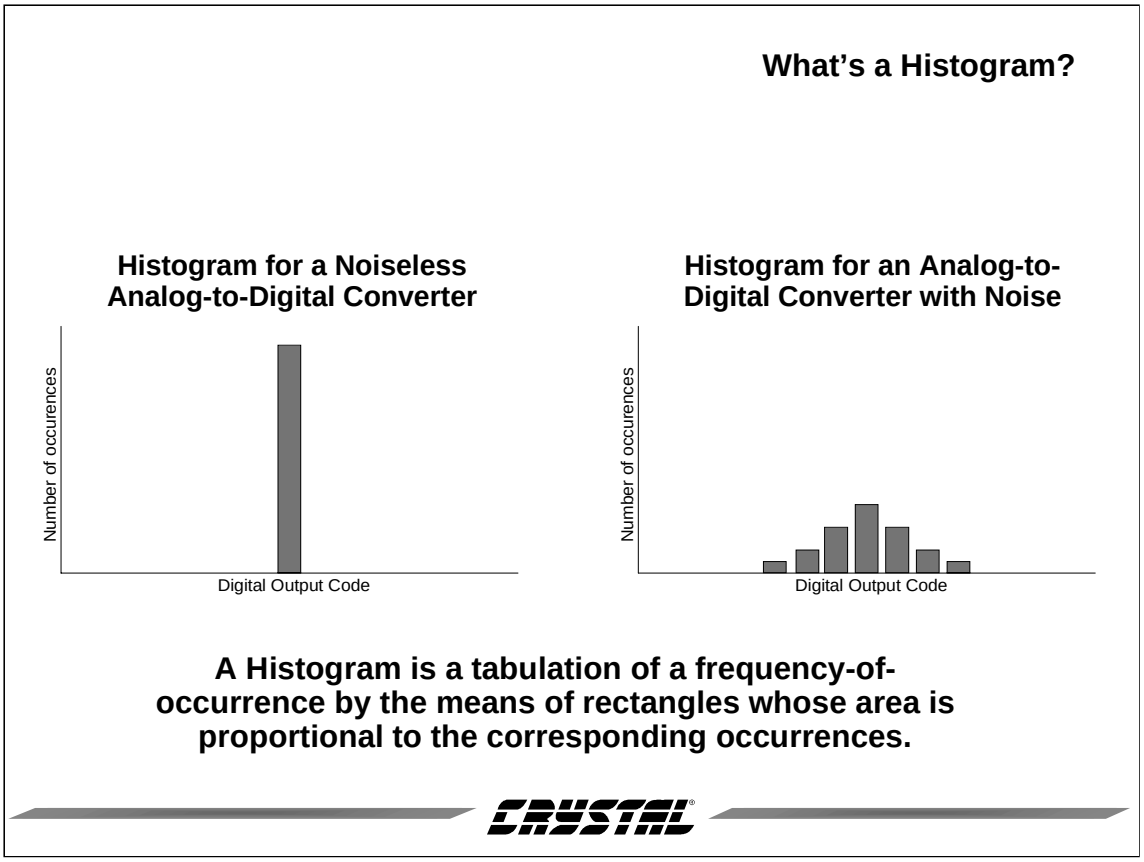
There are specific techniques used to measure and quantify the performance of analog to digital converters and the analog front end. Two basic tests include the use of histograms and Fast Fourier Transforms (FFTs). Each type of test provides a unique perspective of the circuit's performance.

Test selection is based upon the specific parameter measured. For example, histograms are used to measure DC accuracy or static performance characteristics such as offset. FFTs are used to measure dynamic performance characteristics such as linearity. Certain characteristics such as random noise can be measured by either technique.

Combinations of histograms and FFTs can be used for testing and troubleshooting. For example, histograms are used to quantify low level noise and FFTs are used to identify and quantify synchronous noise such as clock feed through. Both tests can use the same data set to determine if the noise is synchronous or asynchronous.

The data illustrated in this section was collected using the Crystal CDBCAPTURE+ interface board and software. The capture interface board is a development tool that interfaces a Crystal Analog-to-Digital Converter (ADC) to a PC-compatible computer. The software provides the capability of time domain, frequency domain, and histogram analysis.

CDBCAPTURE+ is a valuable computer-aided engineering tool which assists in product development and evaluation. It can quantify component and system performance, aiding in system integration. Noise and distortion sources can be identified and performance issues isolated to individual components. The result is a quicker time to market and reduced development costs.



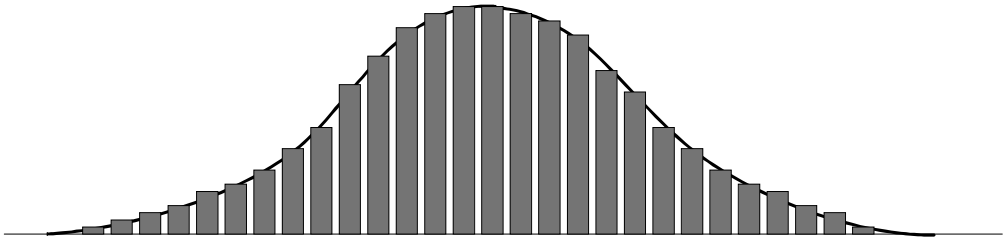
Many analog to digital converters are used to measure the level or magnitude of static signals. Applications include the measurement of weight, pressure and temperature. These applications involve low-level signals which require high resolution and accuracy.

Histograms are used to measure the static performance. A histogram is a tabulation of the frequency of occurrence of a code, and is depicted by the means of rectangles whose area is proportional to the corresponding occurrences. The data from the histograms is used to quantify error and noise associated with the conversion process.

A static input is applied to the Analog-to-Digital Converter (ADC) and multiple output samples are collected. The histogram for a noiseless ADC consists of only one bin, or count, because the output code would be only one value. Every sample collected from a noiseless ADC would be the same value.

If the conversion process has noise added, the values of the sample set will vary according to the amount of noise. The histogram for an ADC with noise will exhibit a distribution of more than one code. The histogram with noise suggests that the output for a static input can be one of seven possible codes.

Estimating the Gaussian Probability Density Function



$$p(x) = \frac{n}{\sigma\sqrt{2\pi}} e^{-(X-\mu)^2/2\sigma^2} \qquad \sigma^2 \approx \frac{\sum_{i=1}^{n}(X_i - \mu)^2}{n-1}$$

$$\mu \approx \frac{1}{n}\sum_{i=1}^{n} X_i$$

Electrical noise resulting from random effects form a Gaussian Distribution. The Gaussian Probability Density Function (p(*x*)) is completely determined with the specification of a mean (μ) and variance (σ^2).

An Analog-to-Digital Converter's (ADC) output varies for a constant input due to noise. The noise is defined by a Probability Density Function (PDF), which represents the probability of discrete events. The PDF's shape describes the certainty of the ADC's output and its noise characteristics.

Statistical techniques are used to acquire performance measurements, assess the effects of noise, as well as compensate for noise. A sample set of data conversions is collected from the ADC and analyzed. The results are used to create a PDF which describes the ADC's true operation.

Electrical noise resulting from random effects forms a Gaussian or normal distribution, which is a bell-shaped curve called a normal curve. The Gaussian PDF is continuous and completely determined with the specification of a mean (μ) and variance (σ2). The Gaussian PDF is defined by the following equation:

$$p(x) = \frac{n}{\sigma\sqrt{2\pi}} e^{-(X-\mu)^2/2\sigma^2}$$

n = 1 for the actual PDF.

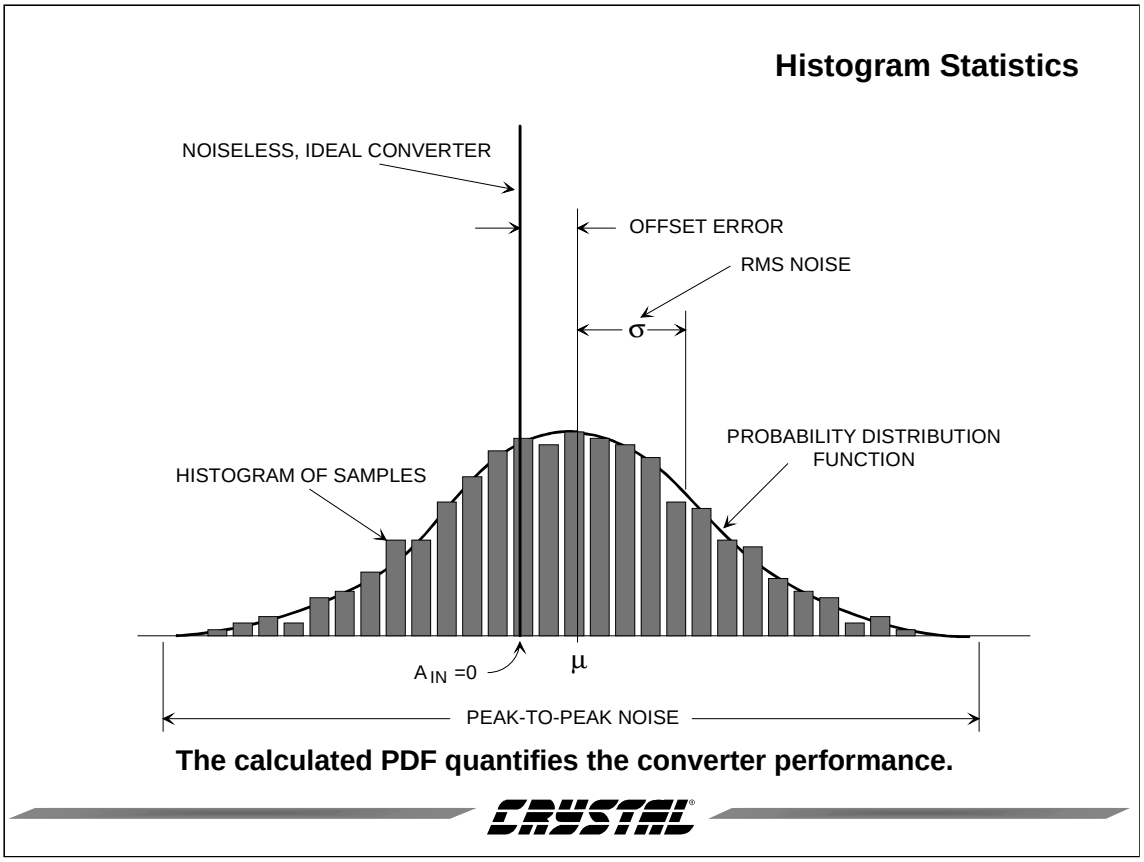
Other values for n scale the PDF to fit a sample set.

The data presented in the histogram can be used to estimate the PDF. The diagram above plots the histogram of an ADC with noise along with its estimated PDF. The mean and variance were estimated from the sample set of data using the following equations.

$$\mu \approx \frac{1}{n}\sum_{i=1}^{n} X_i \qquad \sigma^2 \approx \frac{\sum_{i=1}^{n}(X_i - \mu)^2}{n-1}$$

where X_i is a digital output sample of the ADC and n is the number of samples.

Notice that the PDF and histogram in this example are highly correlated and the estimated PDF seems to be a good model of the actual system.

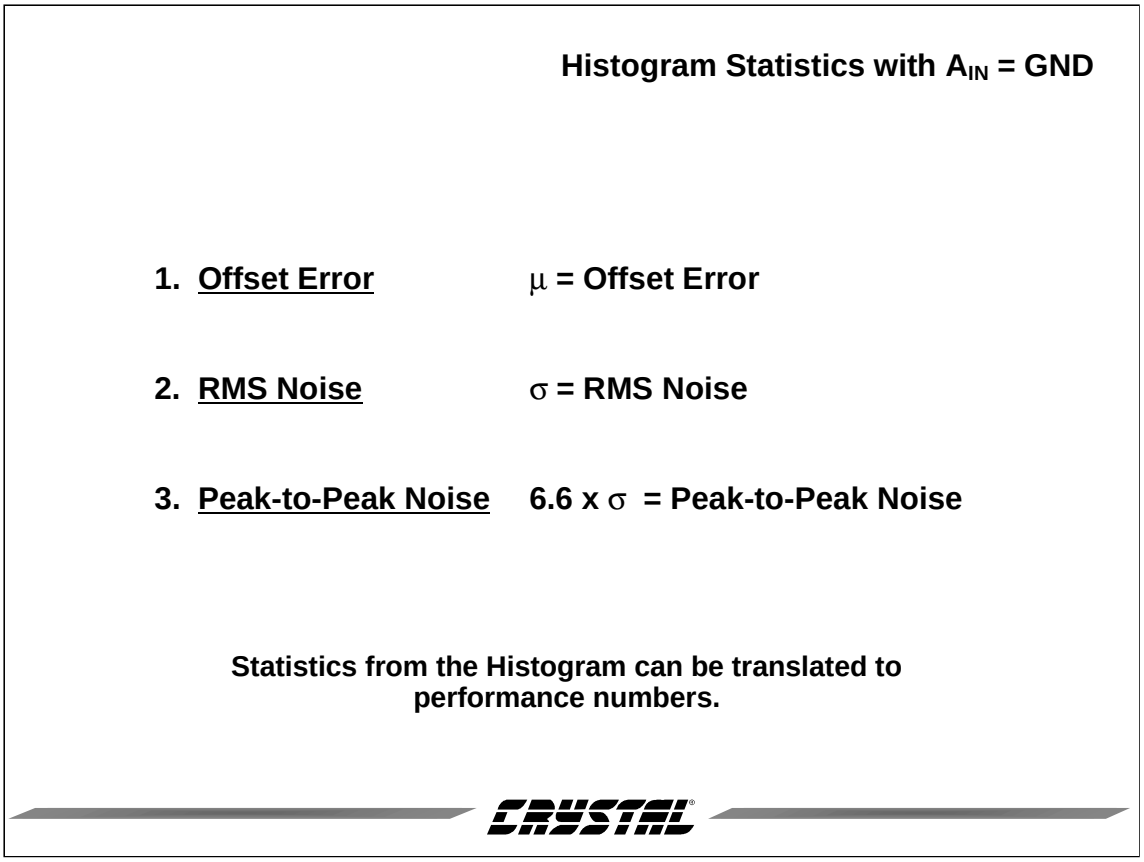


From these Probability Density Function (PDF) parameters, the Analog-to-Digital Converter's (ADC) performance can be quantified. The mean is the expected or average value. It is used to measure offset errors.

The variance describes the variability of the distribution about the mean. It is used as a measurement of uncertainty or noise.

The square root of the variance is called the standard deviation (σ), and it is a measure of the effective or root mean squared (rms) noise. The peak-to-peak noise can be determined from the rms noise value.

When the input to the the ADC is set to zero, the expected digital output is zero. The sample set mean (μ) is the offset error when the the input is set to zero.



Statistics from the histogram are translated to performance numbers. The offset and noise levels are estimated from the sample set of data.

For example, a histogram is made with the data from an Analog-to-Digital Converter (ADC) whose input is grounded. The expected output is zero. The offset error is estimated by the sample set mean. If the offset error is zero, the sample set mean will be zero.

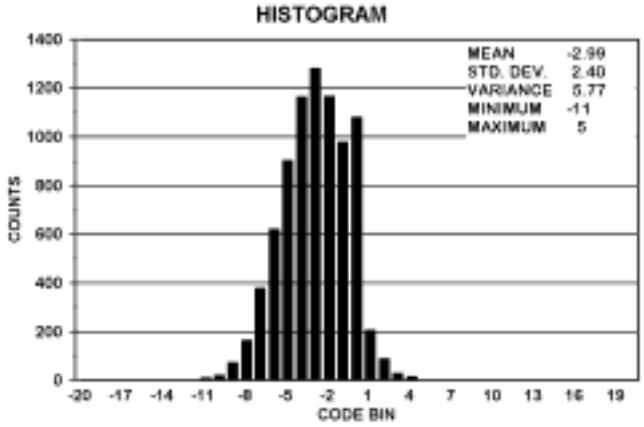
The sample set variance is used to estimate the noise level. The root mean squared (rms) noise is estimated by the standard deviation of the sample set and the peak-to-peak noise is estimated at 6.6 times the rms noise.

In a normal distribution, 6.6 standard deviations contains 99.90% of all occurrences. Numbers other than 6.6 can be used to estimate the peak-to-peak noise. For example 5.0 standard deviations contain 98.8% of all occurrences. The application will dictate the confidence interval.

These calculations can be repeated with different input levels at different points of the ADC's transfer function.

Example of Histogram Statistics using a CS5508

20-BITS **V_{REF} = 2.5V** **A_{IN} = 0V**



Offset Error = -2.99 counts
= -14.3 µV

Noise = 2.40 counts
= 11.4 µV

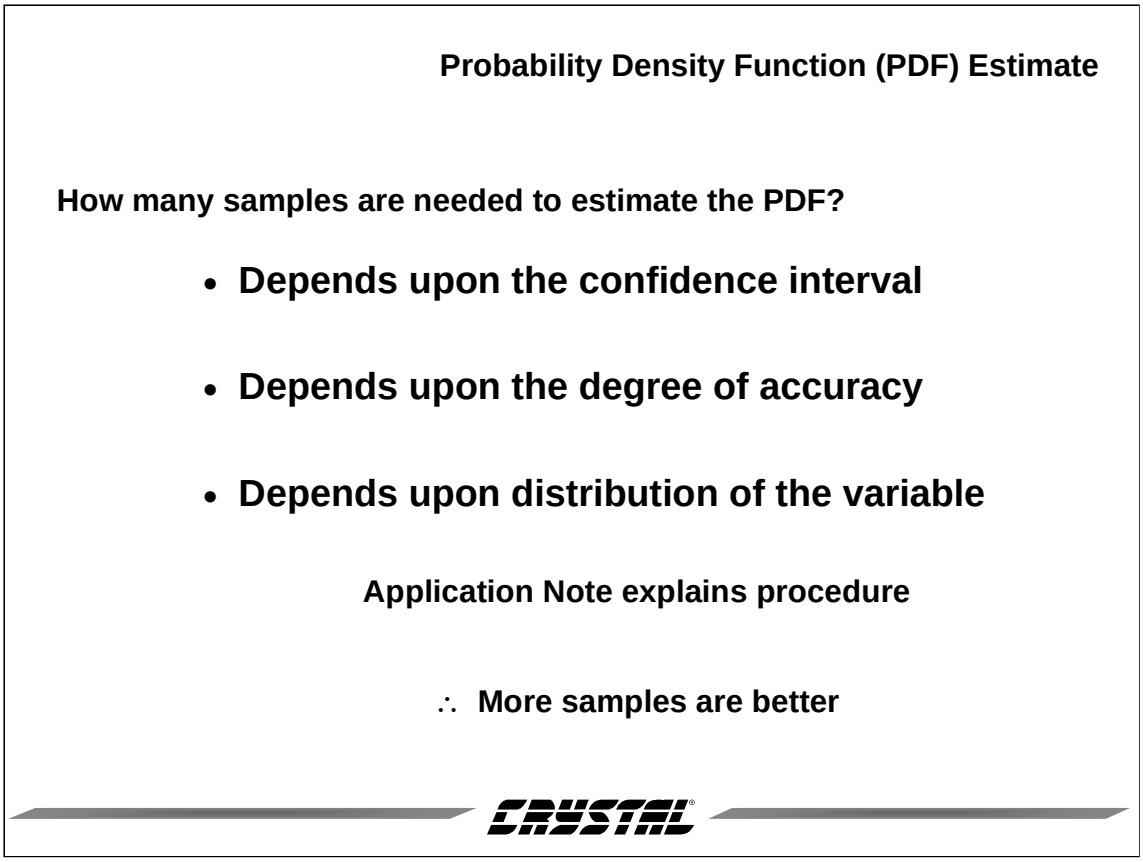
Peak-to-Peak Noise = 6.6 x 2.40
= 15.8 counts
= 75.5 µV

An example of using histogram statistics in measuring the performance of a Cirrus Logic Crystal CS5508. In this case, the CS5508 20-bit Analog-to-Digital Converter (ADC) is used in the bipolar mode with a 2.5 volt reference. The code width (one count) is 4.768 µV under these conditions.

$$4.768\mu V = \frac{(2.5V\ -\ -\ 2.5V)}{2^{20}}$$

8192 samples are collected from the ADC with its input grounded. The offset error is estimated using the sample set mean as being -2.99 counts or -14.3 µV. The rms noise is estimated using the sample set standard deviation as being 2.40 counts or 11.4 µV. Using the sample set standard deviation, the peak-to-peak noise is estimated as 15.8 counts or 75.5 µV.

This test could be repeated with A_{IN} near full scale. In this case, the mean can be used to measure the gain error. The standard deviation or rms noise should remain constant. There may be a difference due to sampling error. A significant increase of the standard deviation indicates noise on the signal source or voltage reference to the ADC.



Previously, the offset error was estimated at -14.7 µV and the noise at 11.4 µV rms. Since these numbers are calculated from sampled data a degree of uncertainty is associated with the estimated performance. The accuracy of the estimate is dependent upon the number of samples collected.

The number of samples that need to be collected depends on several factors including the confidence interval, degree of accuracy and the distribution of the variable.

Confidence interval is the degree of certainty that the estimate is within a specified range. Higher degrees of accuracy or distributions with large variations will require more samples for estimates.

It is generally better to use more samples to calculate estimates for the actual system.

A Cirrus Logic Crystal Application Note, "Noise Histogram Analysis," discusses sampling requirements and uncertainty in greater detail.

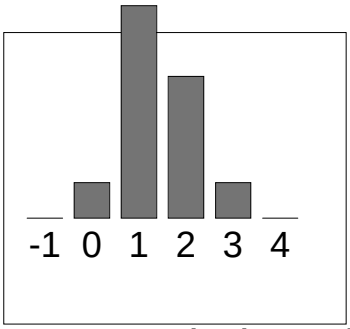
Averaging Multiple Samples

Example:

Set analog input at 1.45 counts

Digital output from the Analog-to-Digital Converter (ADC) :

1, 2, 3, 1, 1, 2, 1, 2, 1, 0, 2, 1



first sample = 1

average first 4 samples = 1.750

average first 9 samples = 1.556

average 12 samples = 1.417

Averaging is a method used to increase the resolution of an ADC and decrease the uncertainty due to noise.

Averaging is a method used to increase the resolution of an Analog-to-Digital Converter (ADC) and decrease the uncertainty due to noise.

In the example above, the input to the ADC is equivalent to 1.45 counts. The output of the ADC would always be 1 if no noise were present. However, noise is present and twelve output samples from the ADC are 1,2,3,1,1,2,1,2,1,0,2,1.

If only one sample from the ADC is used, the sample could be any one of four possibilities ranging from 0 to 3. For example, if only the first sample is used, the result is 1.

Multiple samples can be averaged to increase the accuracy. If the first four samples are averaged the result is 1.750, averaging nine samples gives a result of 1.556, and averaging all 12 samples results in 1.417. Notice how using more samples produces a result which is closer to the actual value of 1.45 counts. Averaging increase the precision of the conversion.

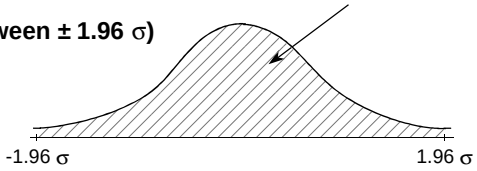
Q: How accurate is the result of averaging?

A: The uncertainty depends upon the sample set's variance.

Example: **RMS noise = σ**

Confidence interval = 95%
(95% of occurrences are between ± 1.96 σ)

95% of Total Area



μ = 1.417 σ^2 = 0.629 σ = 0.793

		Average		Uncertainty	
1	**sample**	**1**	**±**	**1.554**	**where 1.554 = (1.96)(0.793)**
4	**samples**	**1.750**	**±**	**0.777**	**where 0.777 =** $1554 / \sqrt{4}$
9	**samples**	**1.556**	**±**	**0.518**	**where 0.518 =** $1554 / \sqrt{9}$
12	**samples**	**1.417**	**±**	**0.449**	**where 0.449 =** $1554 / \sqrt{12}$

Averaging reduces uncertainty by $1/\sqrt{\text{number of averages}}$

As discussed in the "Noise Histogram Analysis" Application Note, the accuracy of averaging and the uncertainty associated with sampled data depends upon the sample set's variance.

Uncertainty can be calculated. From the previous example, the sample set of 12 has the following statistics:

sample mean = 1.417
sample variance = 0.629
sample standard deviation = 0.793

The statistical characteristics of a normal distribution state that 95% of all occurrences will be within ±1.96 standard deviations. Using one sample, the variation is ±(1.96 * 0.793) or ±1.554 counts. If the Analog-to-Digital Converter (ADC) output is 1, there is a 95% certainty that the actual value is between -0.554 and 2.554.

Averaging multiple samples reduces the standard deviation of the averaged data set by 1 over the square root of the number of samples. Using the example sample set, averaging 12 samples results in 1.417 counts with an uncertainty of ±0.449 counts. the uncertainty was reduced by $\frac{1}{\sqrt{12}}$. Averaging improves the accuracy of the conversion.

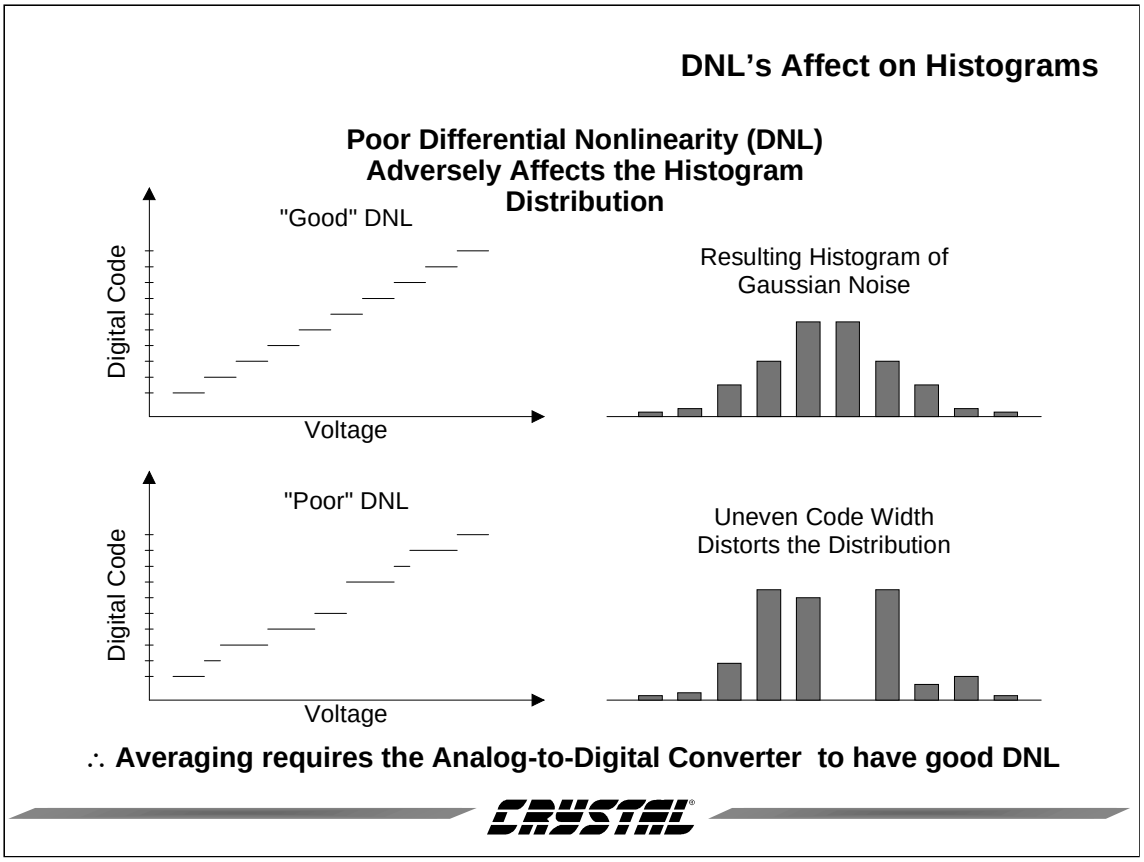
Averaging can improve the resolution of an ADC. If enough samples from a 16-bit ADC are averaged together, the result can be accurate to a 17-bit or 18-bit resolution.

Quantization produces an uncertainty of ±0.5 counts.

If one sample is used (no averaging), the uncertainty is ±1.554 counts. The total uncertainty is 3.108 counts. If the ADC has a resolution of 16-bits, the effective resolution is between 14 and 15 bits noise free.

If 12 samples are averaged together, the uncertainty is reduced to ±0.449 counts or a total uncertainty 0.898 counts. The total uncertainty of a noiseless converter is 1.0 count due to quantization error. Averaging 12 samples from a 16-bit ADC provides slightly better than 16 bits of noise free resolution.

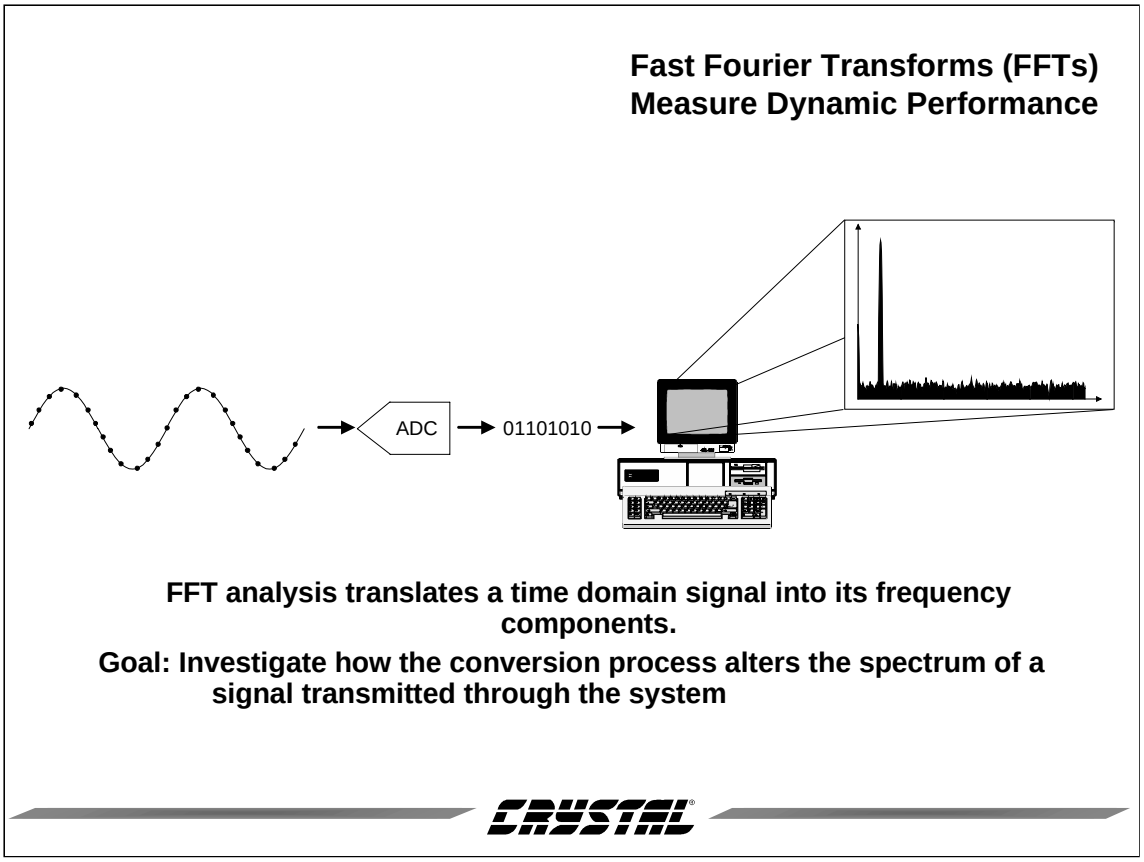
If 39 samples are averaged together, the uncertainty is reduced to ±0.249 counts. The total uncertainty is less than a 0.5 counts. The result of averaging 39 samples is better than 17 bits of noise free resolution.



Poor Differential Nonlinearity (DNL) adversely affects the histogram distribution. This point is very important. In the histogram calculations, it is assumed that the uncertainty is a result of random noise and the sample set possesses a normal or bell-shaped distribution.

Poor DNL distorts the distribution of random noise. Wide codes have a higher probability of occurrence than narrow codes. DNL error affects the histogram distribution.

If the distribution is severely distorted, the statistics may be unreliable. It is important to choose an Analog-to-Digital Converter (ADC) with good DNL characteristics if the application requires averaging.

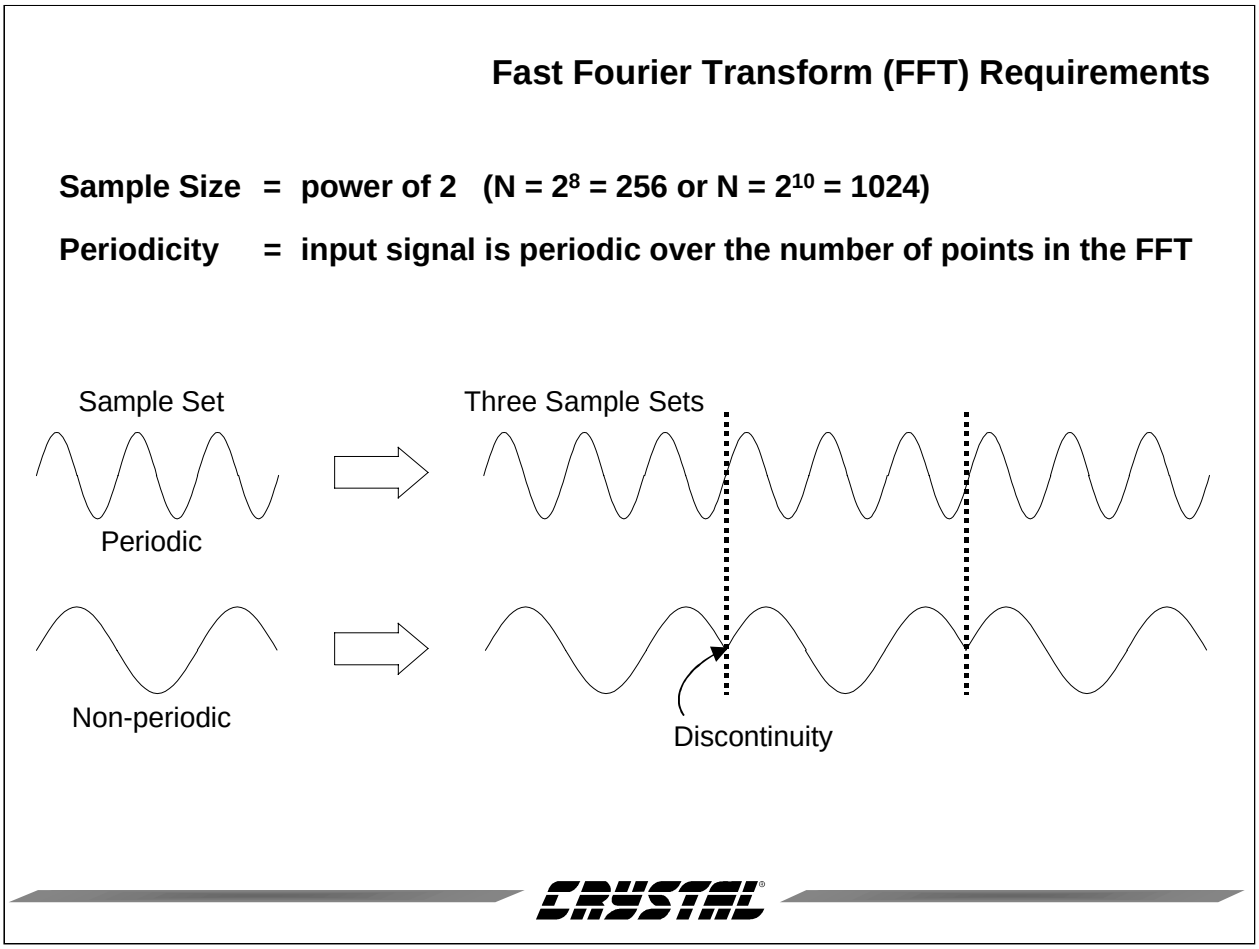


The rapid growth of digital signal processing applications has resulted in the need for Analog to Digital Converters (ADCs) to be tested using dynamic signals.

In measuring an ADC's dynamic performance, the goal is to investigate how the conversion function alters the spectrum of a signal transmitted through the system. Spectral analysis is used to find the frequency content of signals. Here, time domain signals are transformed to the frequency domain. The magnitude portions of the frequency elements are used to determine the signal power distribution with respect to frequency, by constructing a power spectrum plot. The power spectrum is used for measuring system distortion, dynamic range, attenuation, and induced noise.

Frequency domain analysis begins with the translation of a time domain signal into its frequency elements. The frequency elements consist of magnitude and phase components.

Applications using frequency domain information include Radar, Sonar, Speech Recognition, Vibration Analysis, Video Inspection, Medical Imaging, and Instrument Control. Specific applications emphasize analyzing certain information of the frequency components. For example, range finding radar uses the phase information of the transmitted signal and its received reflections. The phase difference between the transmitted and received signals contains range information. For quantifying ADC performance, only the magnitude component is used.

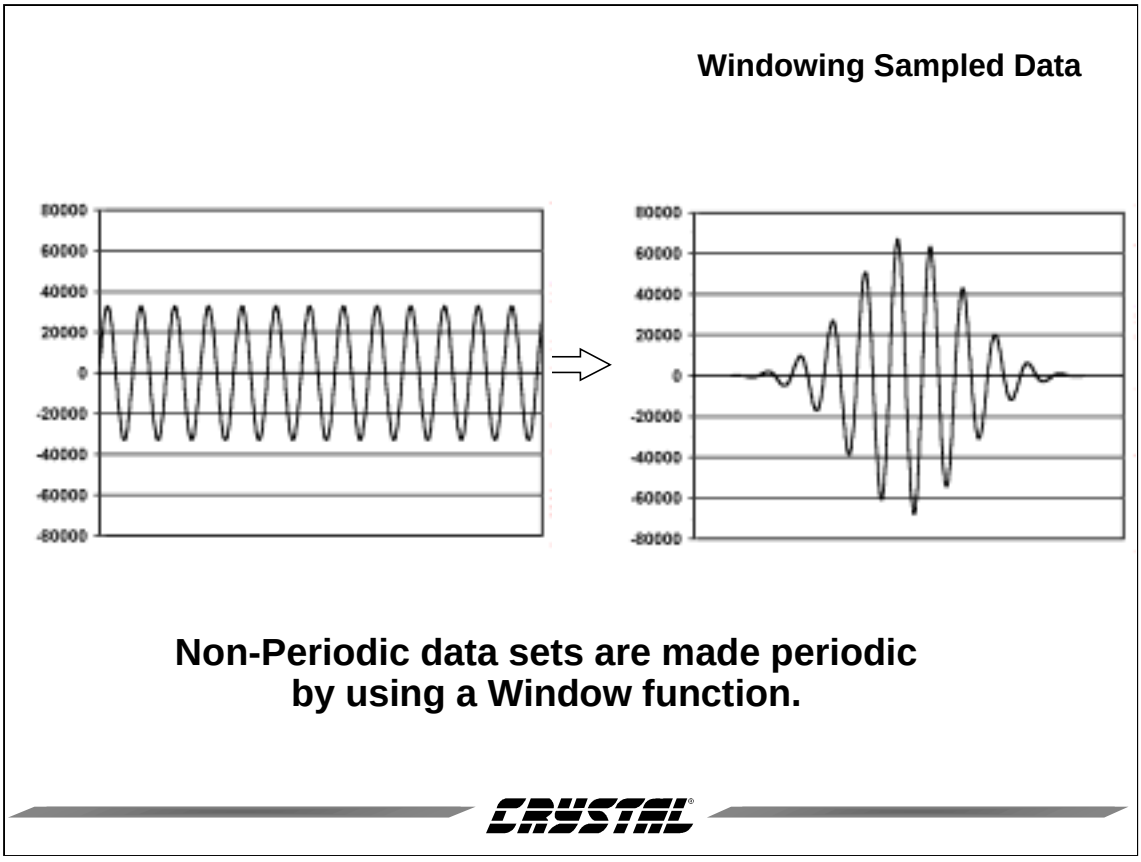


The Fast Fourier Transform (FFT) process starts at the Analog-to-Digital Converter (ADC), which converts a continuous analog signal to a discrete digital representation (sampling). The analog signal's amplitude is converted to an n-bit binary representation called a digital word. The ADC outputs these digital words at a rate set by the sample frequency (F_S). This sample frequency is primarily determined by the ADC's throughput.

A sample set of data points is collected for the FFT algorithm. The FFT algorithm operates on a set of N samples, for which N must be a power of 2 (for example, $N=2^8=256$ or $N=2^9=512$). The sample set size is determined by the processing capability (computer memory size and processing throughput), input signal dynamics, and degree of frequency resolution.

The FFT algorithm assumes that the input signal is periodic over the number of points in the FFT. This means that multiple copies of the signal can be placed end to end without any discontinuities at the points which they meet. The "FFT Requirements" diagram displays a signal that is periodic for the number of points in the FFT. The first sample set illustrates periodicity, when 3 sets of data are combined, there are no discontinuities (smooth transitions between sample sets).

The second sample set illustrates a signal that is non-periodic for the number of sample points and highlights the discontinuities at the points where copies meet. An FFT of the non-periodic data will result in high frequency elements that do not exist in the actual signal.

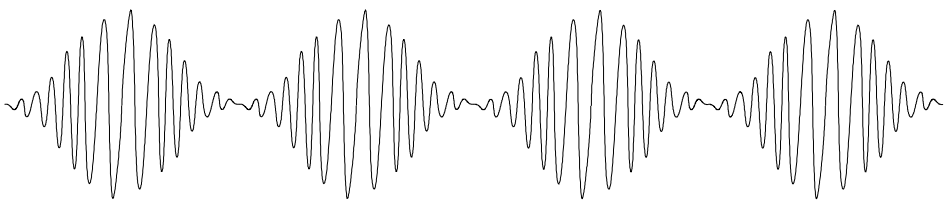


The Fast Fourier Transform (FFT) algorithm's periodicity requirement that the sample set contain an integer number of signal cycles is not practical for most applications. This in effect makes Fs and N functions of the input frequency. Periodicity is further complicated when the input signal is composed of multiple frequency elements or is not a pure sine wave.

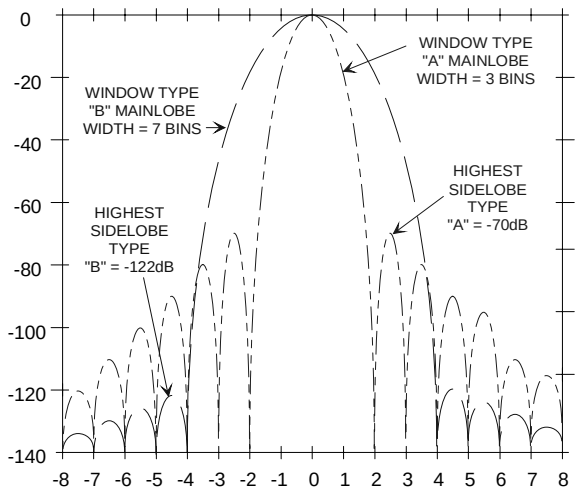
Windows are used to reduce the spectral leakage that results from using the FFT on a non-periodic or dynamic signals. "Windowing" multiplies the time domain signal by a function that attenuates the amplitude on the ends, thus reducing the discontinuities. The windowed data sets can be combined without any discontinuities.

The affect of windowing data is that sinusoidal energy is spread from one bin to several bins within the mainlobe and sidelobes.

The goal in window selection for dynamic measurements is to keep the fundamental energy in the mainlobe and have negligible leakage to the sidelobes.



Window Effects



	Mainlobe Width	Highest Sidelobe
Type “A”	3 Bins	-70 dB
Type “B”	7 Bins	-122 dB

When using a window function, the primary tradeoff is between smearing the input signal among several bins and dealing with sidelobes.

With window functions, the primary tradeoff is between smearing the input signal among several bins and dealing with sidelobes. Frequency resolution and spectral leakage are influenced by the choice of window function.

When using a window, the input signal is spread among the frequency bins which represent the mainlobe, thus the exact frequency is less sharply defined. A wide mainlobe produces greater signal smearing than a narrow mainlobe.

The degree of signal leakage to bins outside the mainlobe is dependent upon the magnitude of the sidelobes. If the sidelobe level is higher than the noise floor, the input signal leaks to frequencies outside the mainlobe. Sidelobe magnitude is generally inversely proportional to the width of the mainlobe. Thus, lesser frequency resolution is traded off for better sidelobe attenuation.

In the above diagram, the mainlobe’s width for the type "A" window is three bins and highest sidelobe is -70 dB. Type "B" window’s highest sidelobe is -122 dB, which is 55 dB better than type "A". The improvement in sidelobe attenuation resulted in a mainlobe width of seven bins, an increase of four bins.

The window’s rise/fall time and width characterize the window performance. Rise/fall time is the rate of endpoint attenuation. A fast rise/fall time produces high sidelobe levels. The width of the window is the number of samples where the window is at its maximum value. The mainlobe width is inversely proportional to the window width. A large window width creates a small mainlobe width. When the width of the window is lengthened to decrease the mainlobe width, the rise/fall time increase, resulting in higher sidelobes.

Five Types of Windows

Window Type	Mainlobe Width (BINS)	Highest Sidelobe Level (dB)
Hanning	5	-32
Blackman	7	-58
Minimum 4-Term Blackman-Harris	9	-92
5-Term HODIE	11	-125
7-Term HODIE	15	-175

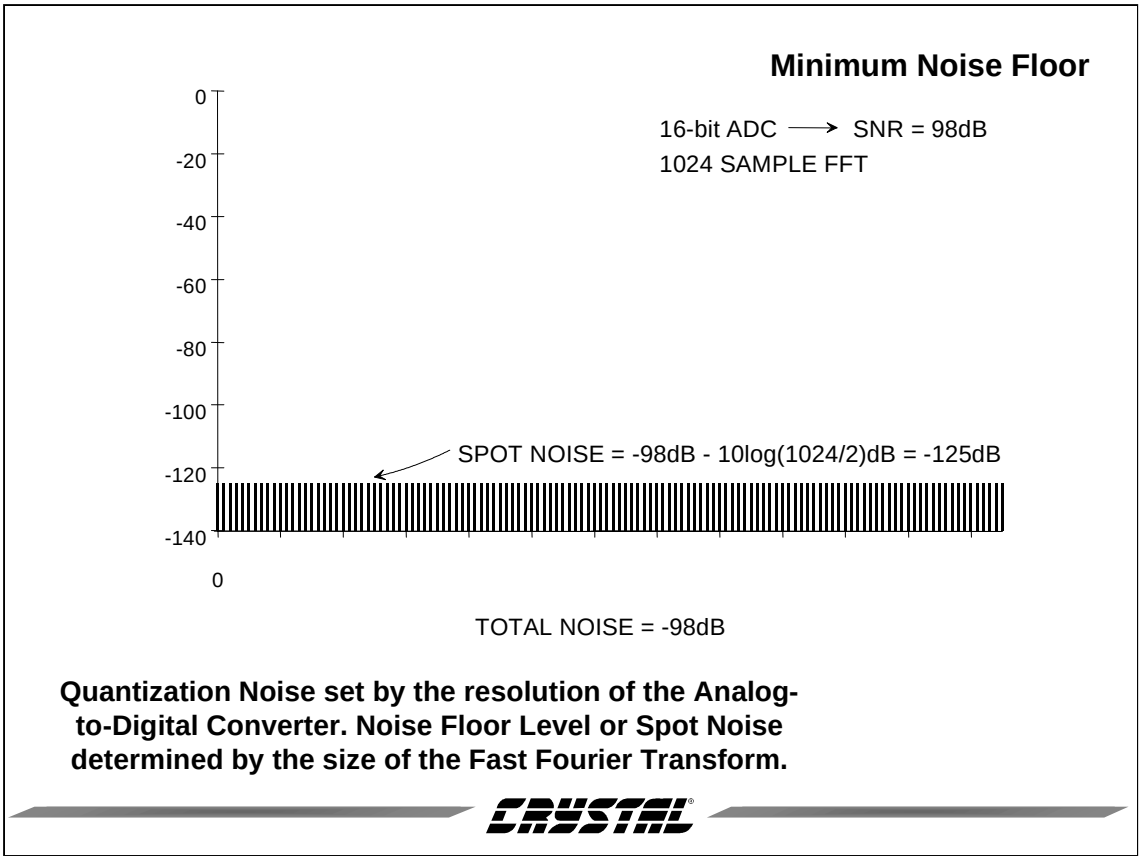
Notice tradeoff between mainlobe width and highest sidelobe.

Choosing the appropriate window depends upon the application, system performance, and the information required. A window function's figure of merit include: Highest Sidelobe level, Sidelobe fall-off, Equivalent Noise Band Width, 3 dB Band Width, Scallop loss, and Worst Case Process loss. These measurements are discussed in "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform." by F.J. Harris, Journal of the IEEE, Vol. 66, No.1, Jan 1978.

Measuring the performance of an Analog-to-Digital Converter (ADC) system is a typical application for Fast Fourier Transform (FFT) analysis. The goal is to obtain a power spectrum of a pure sine wave input. A pure sine wave is a periodic or stationary signal and is composed of only one frequency and constant amplitude. The use of a pure sine wave reduces the number of variables and permits accurate measurement of system performance.

The goal is to keep all the signal power in the mainlobe. This requires that the window function's sidelobes be lower than the theoretical noise floor. The low sidelobes reduce the spectral leakage to bins outside the mainlobe, making the computation of signal power easier.

The width of the mainlobe and highest sidelobe level for the five windows are listed in the "Window Type". Note the tradeoff between mainlobe width and sidelobe level.



In measuring dynamic performance, calculations are easiest when a window's sidelobes are below the minimum noise floor. This results in the noise floor's shape being dictated by the Analog-to-Digital Converter's (ADC) performance.

The minimum noise floor is set by the ADC's resolution and the number of samples used in the Fast Fourier Transform (FFT). The following illustrates the calculation of the spot noise for an ideal 16-bit ADC and a 1024 sample FFT. Using the following formula, Signal-to-Noise Ratio (SNR) is 98.08 dB.

$$SNR = 6.02N + 1.76\,(dB)$$

The noise floor is determined by the quantization error and is 98.08 dB less than a full scale signal. In a 1024 sample FFT, there are 512 bins between zero and the Nyquist frequency. The quantization error is spread evenly among 512 bins.

$$Spot\,Noise = -98.08 - 10\log(512) = -125dB$$

A formula for spot noise as a function of ADC resolution and FFT sample size is:

$$Spot\,Noise = -6.02N - 176 - 10\log\left(\frac{samples}{2}\right)dB$$

Noise Floors for Ideal Analog-to-Digital Converters

Number of Bits Resolution	Number of Samples	Average Spot Noise
12	256	-95
14	256	-107
16	256	-119
12	1024	-101
14	1024	-113
16	1024	-125

Average Spot Noise = Noise floor level for an ideal ADC

The highest sidelobe level must be less than the average spot noise.

Example: 16-bit ADC, 1024 samples $\Longrightarrow$ 5-Term HODIE or 7-Term HODIE

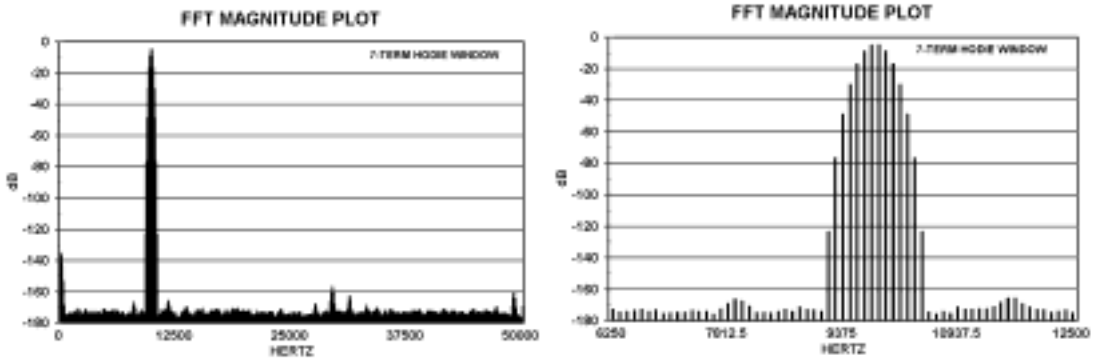
The noise floor for an ideal Analog-to-Digital Converter (ADC), which is used to select the appropriate window type, is set by quantization error and the number of samples.

A 16-bit ADC and 1024 samples sets the theoretical noise floor at -125 dB. This is based upon quantization error and sample number.

The windowing algorithm used must attenuate the sidelobes below -125 dB. Using the results from the "Window Type" table, the HODIE 5-term or HODIE 7-term window is required to concentrate all the signal power in the mainlobe. The other three windows leak signal power to the sidelobes.

Appropriate Window

ADC Resolution = 24 Bits
Sample Size = 1024
Average Spot Noise at -173 dB



Noise Floor Shape determined by Analog-to-Digital Converter

Mainlobe width = 14 Bins

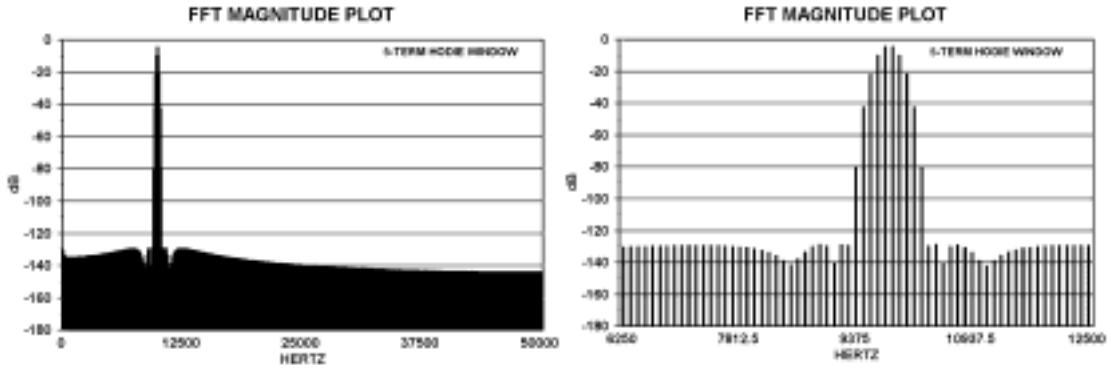
Signal power is concentrated in mainlobe

This example involves selecting a window to measure the dynamic performance of a 24-bit Analog-to-Digital Converter when performing a 1024 sample Fast Fourier Transform (FFT). The spot noise is calculated to be greater than -173 dB. Thus the highest sidelobe should be less than -173 dB.

The HODIE 7-term window is suitable for this application. Notice that the shape of the FFT's noise floor is set by the ADC's characteristics.

High Sidelobe Window

Analog-to-Digital Converter Resolution = 24 Bits
Sample Size = 1024
Average Spot Noise at -173 dB



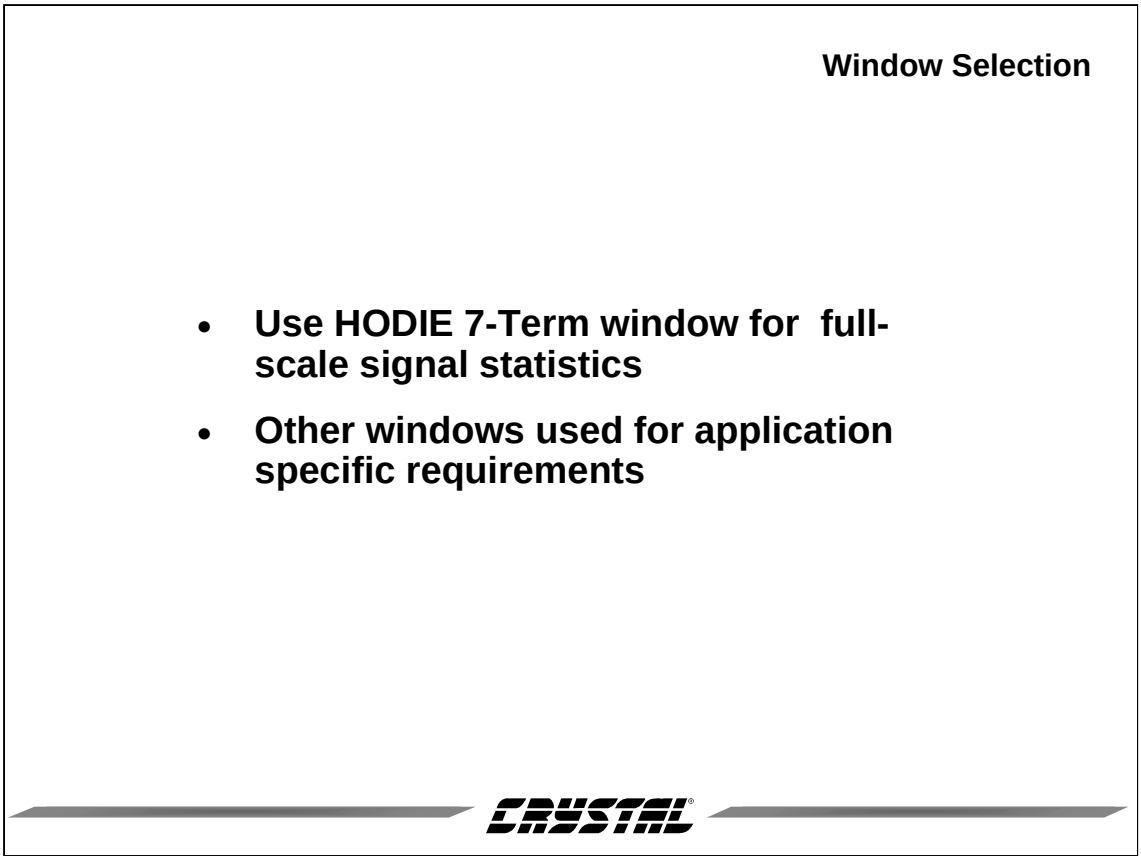
Noise Floor Shape determined by Window

Mainlobe Width = 10 Bins

Signal power is leaked to the sidelobes

The HODIE 5-term window would not be adequate for this application due to it's high sidelobes. Notice how a full scale signal's energy has leaked out of the mainlobe and spread to the sidelobes.

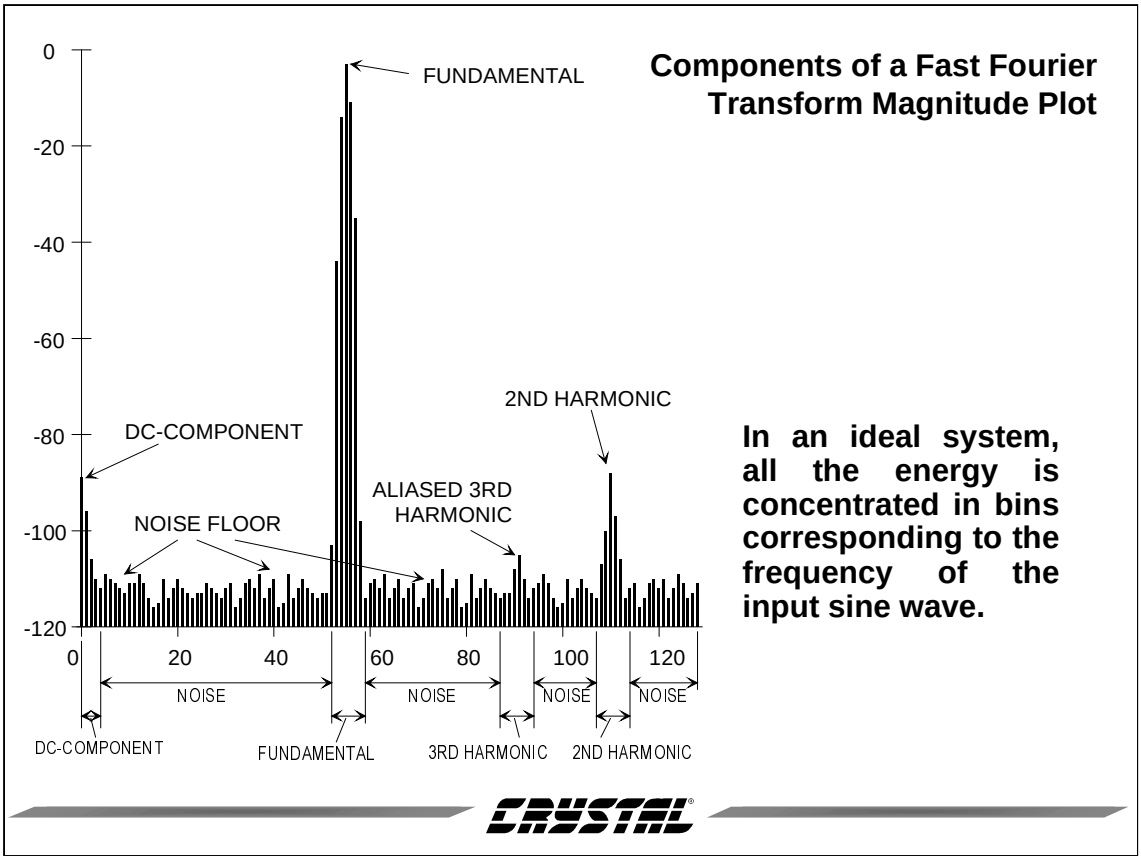
The noise floor shape is determined by the window characteristics.



The HODIE 7-term window should be used for acquiring statistical measurements when a full scale input signal is applied to the Analog-to-Digital Converter (ADC). This will reduce the affect of signal energy leaking to the sidelobes. The HODIE 7-term window is appropriate use with any Cirrus Logic Crystal ADC.

Other windowing algorithms are included with the CDBCAPTURE system. These windows are used in applications where the sidelobe height is unimportant. Examples include of cases where analog input signals are less than full scale, synchronous sampling applications, and signal detection.

As a rule of thumb, when measuring the performance of an Analog-to-Digital Converter with a full scale input signal, use the HODIE 7-term window.

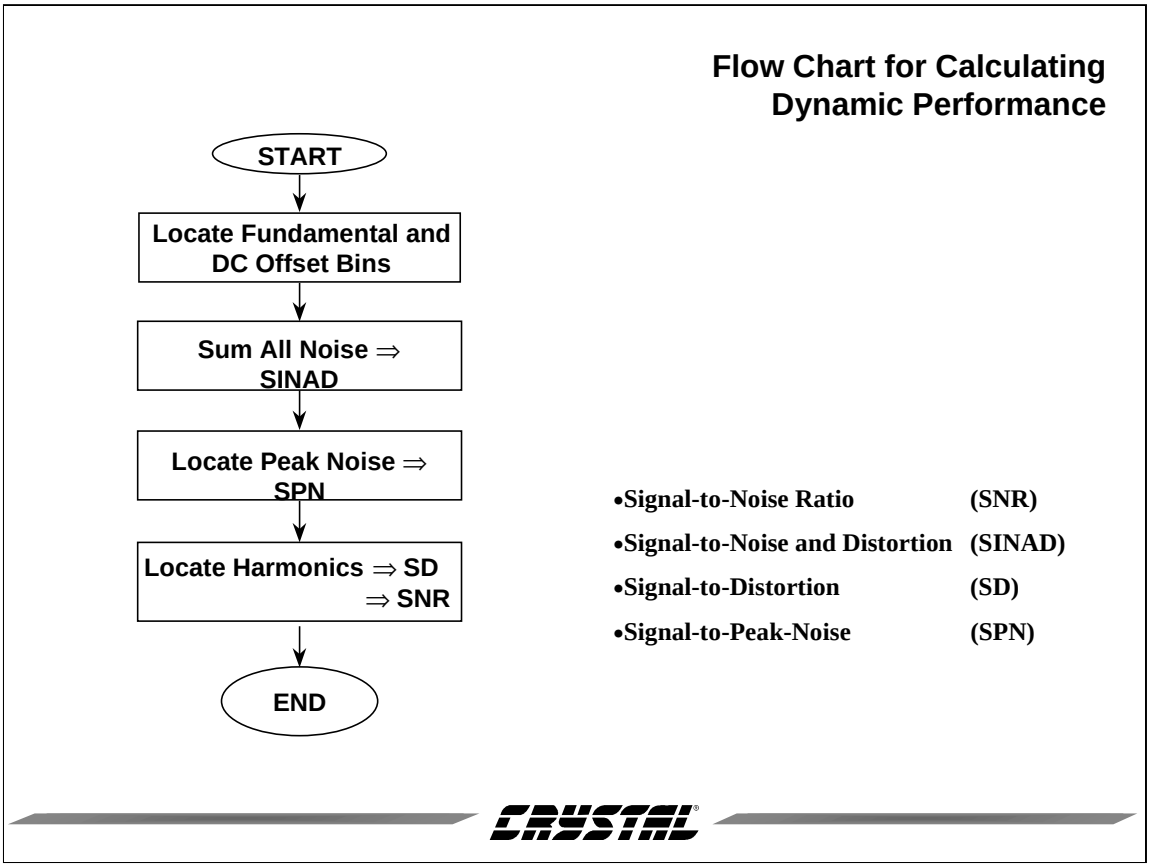


Quantitative measurements of system performance can be made from the results presented in a power spectrum. The power spectrum illustrates the spectral density of the measured signal which can show the corruption of a pure sine wave by an electronic system. In a perfect system, all the signal energy is concentrated in bins corresponding to the frequency of the input sine wave. The noise floor of the power spectrum will be flat and at a level corresponding to the number of bits of resolution used by the Analog-to-Digital Converter (ADC) (quantization error). Ratios quantify the ADC's performance by measuring how a signal is corrupted with noise and distortion.

Above is a power spectrum obtained from a 256 sample (N=256) Fast Fourier Transform (FFT). The ADC's sample rate is 256 Hz (F_s = 256 Hz.). Each bin on the x-axis represents a 1 Hertz band of power. A full-scale, 55.1 Hz sinusoid is applied to the ADC. After 256 samples are collected, the data set is multiplied by a window whose mainlobe width is seven bins and highest sidelobe is less than -120 dB.

The y-axis represents the power concentrated in the frequency range represented by each bin. Power is plotted in terms of decibels (dB), and the ratio is taken with respect to the signal power of a full scale sinusoid.

The power spectrum can be divided into various subsections which include the Fundamental, Secondary Harmonics, DC-Component, and Noise Floor. The power for each of these sections are calculated. The power numbers are used in calculating the signal to noise ratios used to quantify performance.



Four key performance measurements can be calculated from the power spectrum obtained from an Fast Fourier Transform (FFT): Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion (SINAD), Signal-to-Distortion (SDR), and Signal-to-Peak-Noise (SPN). Each parameter gives insight to the system's linearity and noise characteristics. They are used in benchmarking performance or identifying specific performance issues.

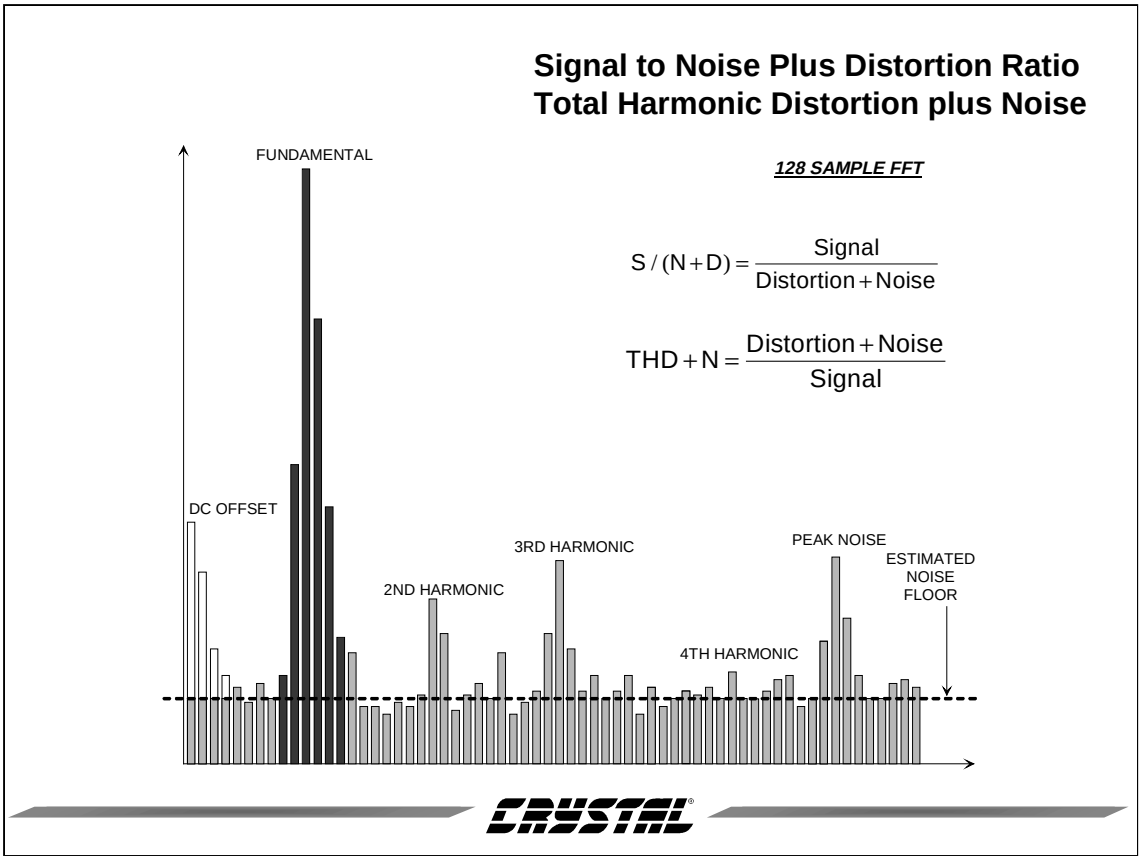
With the power spectrum constructed, the dynamic performance statistics can be calculated. An algorithm is used to identify the various subsections of the power spectrum. First the spectrum is searched for the highest bin, locating the fundamental signal. The power of the fundamental signal is calculated with consideration for the the type of windowing algorithm used.

The next section identified is the DC offset bins. The size of this area depends upon the windowing algorithm used. The DC offset is not used in measuring dynamic performance.

With the fundamental and DC-offset sections identified, the power in the remaining bins are summed and a ratio determined versus the fundamental signal power. This ratio is the SINAD value.

The next step is to locate the second highest bin outside the fundamental and DC offset areas. This bin locates the area of peak noise. The power in the peak noise signal is calculated and the SPN ratio obtained.

The last step is to locate the secondary harmonics associated with the fundamental signal. Here the algorithm searches the spectrum for non-aliased and aliased harmonics. The power associated with the secondary harmonics is considered distortion. Calculating the distortion power leads to obtaining SD and SNR ratios.



SIGNAL to NOISE and DISTORTION (SINAD):

Signal to Noise and Distortion is a measure of the broad band noise and distortion introduced into the signal. The rms magnitude of the input sine wave is compared to the sum of all other frequencies, except the DC-component. The ratio of the input signal to the sum of the individual noise and harmonic components is expressed in terms of decibels (dB). The higher the SINAD figure, the better the general performance.

Total Harmonic Distortion plus Noise (THD+N):

Total Harmonic Distortion plus noise is similar to SINAD except the numerator and denominator are switched. THD+N is often used in audio applications as a single figure of merit in quantifying performance and is expressed either in terms of percentage (%) or decibels (dB).

% vs. dB Representation

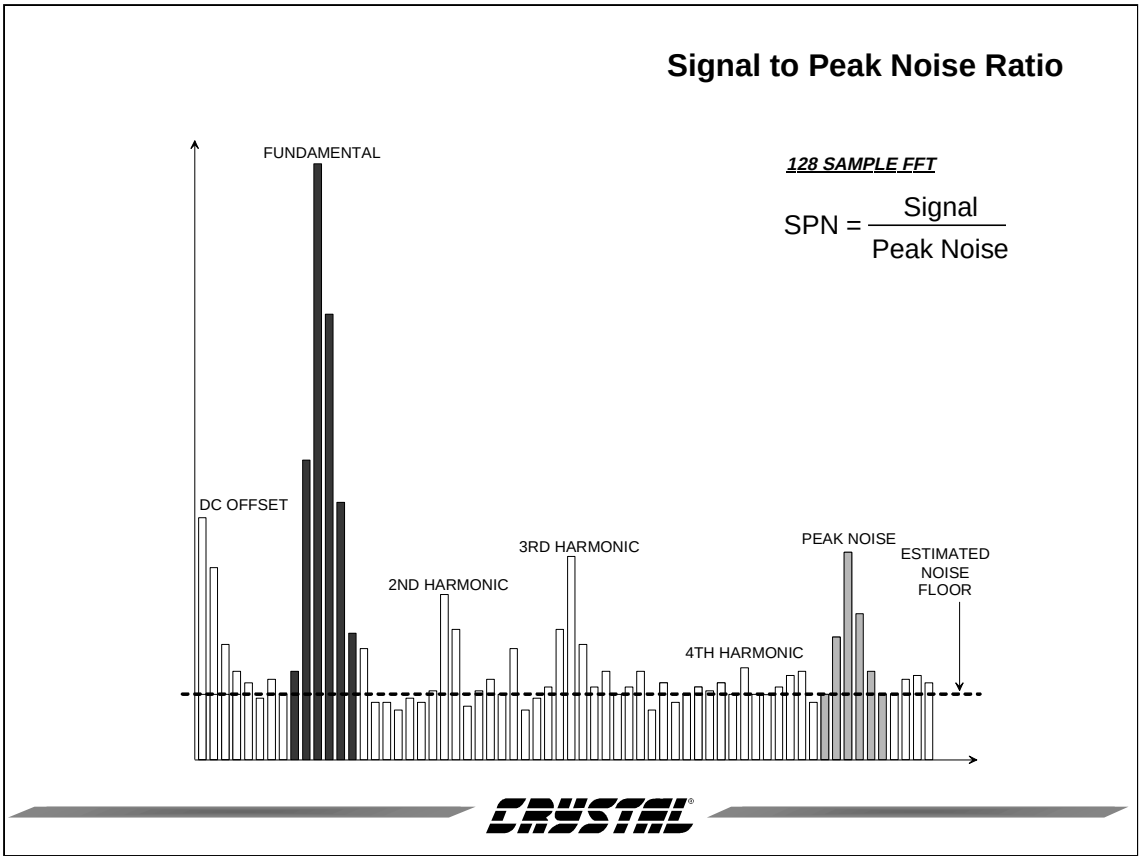
% THD+N = (THD+N) x 100%

THD+N (dB) = 20 log(THD+N)

example:

THD+N

	(typical)	(maximum)
	-100 dB	-94 dB
	0.001%	0.002%

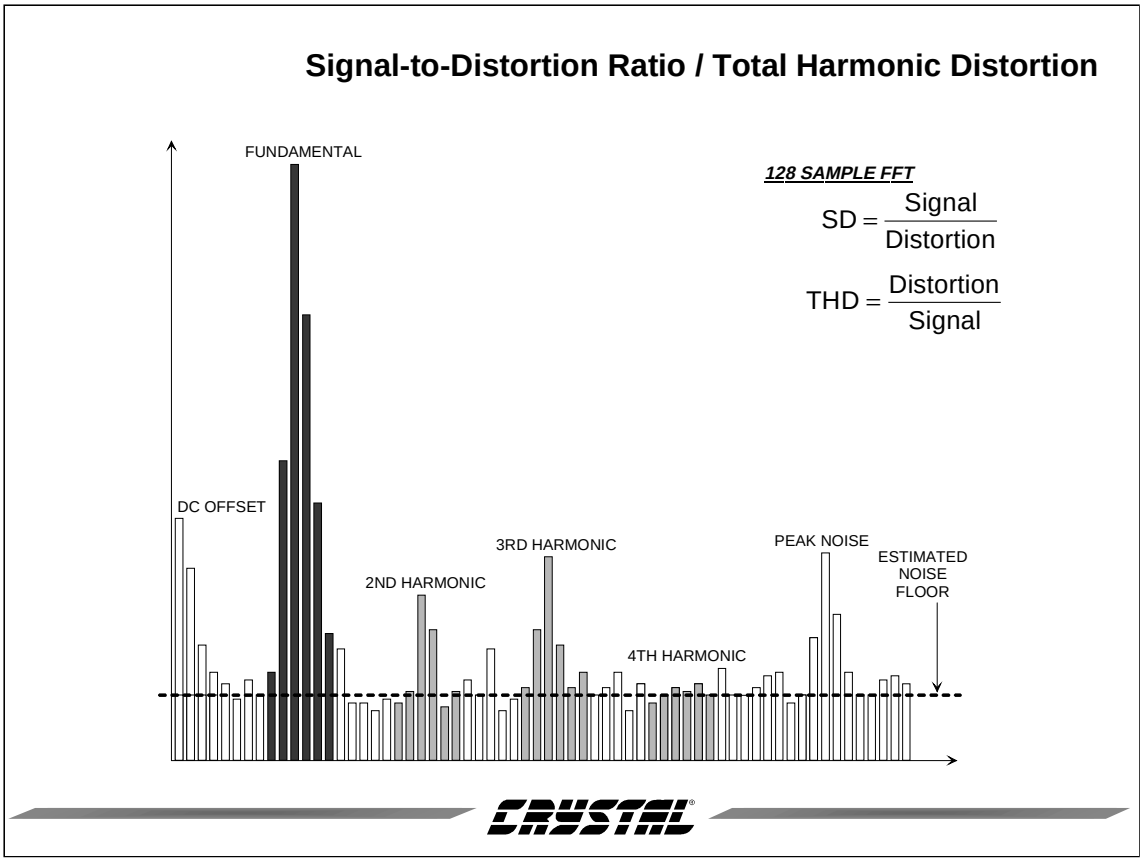


SIGNAL-to-PEAK NOISE (SPN):

Signal-to-Peak Noise is a measure of the highest noise or distortion component introduced into the signal. The highest noise or distortion component determines the lowest level of a signal that can be detected.

The rms magnitude of the input signal is compared to the rms magnitude of the highest noise or distortion component.

The ratio of the input signal to the peak noises component is expressed in terms of decibels (dB). The higher the SPN value, the better the detectability of low level signals.

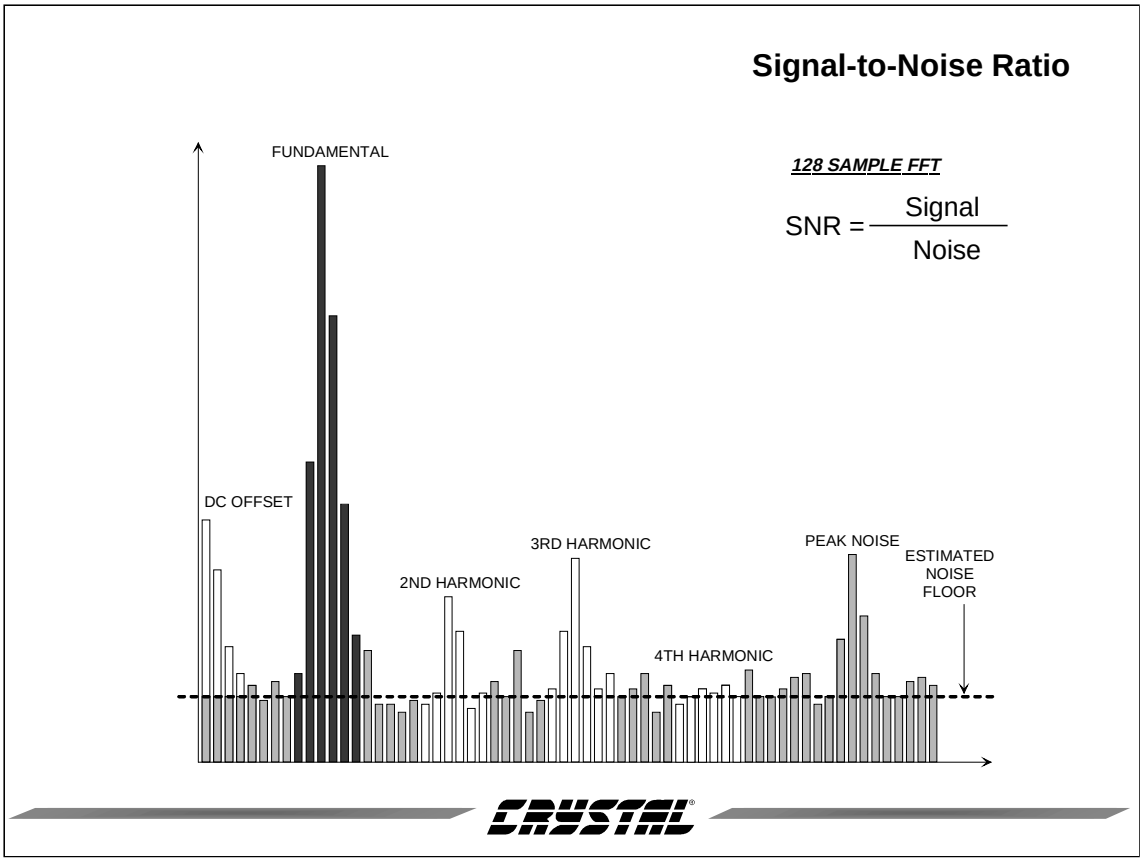


SIGNAL-to-DISTORTION RATIO (SDR):

Signal-to-Distortion is a measure of the harmonic distortion introduced into the signal. The harmonic distortion degrades the fidelity of the measured signal. A good signal-to-distortion figure suggests good integral non-linearity (INL). The rms magnitude of the input signal is compared to the sum of the harmonic components (signals at integer multiples of the input signal frequency). The ratio of the input signal to the sum of the harmonic components is expressed in terms of decibels (dB). The higher the SDR value, the higher the fidelity.

TOTAL HARMONIC DISTORTION (THD):

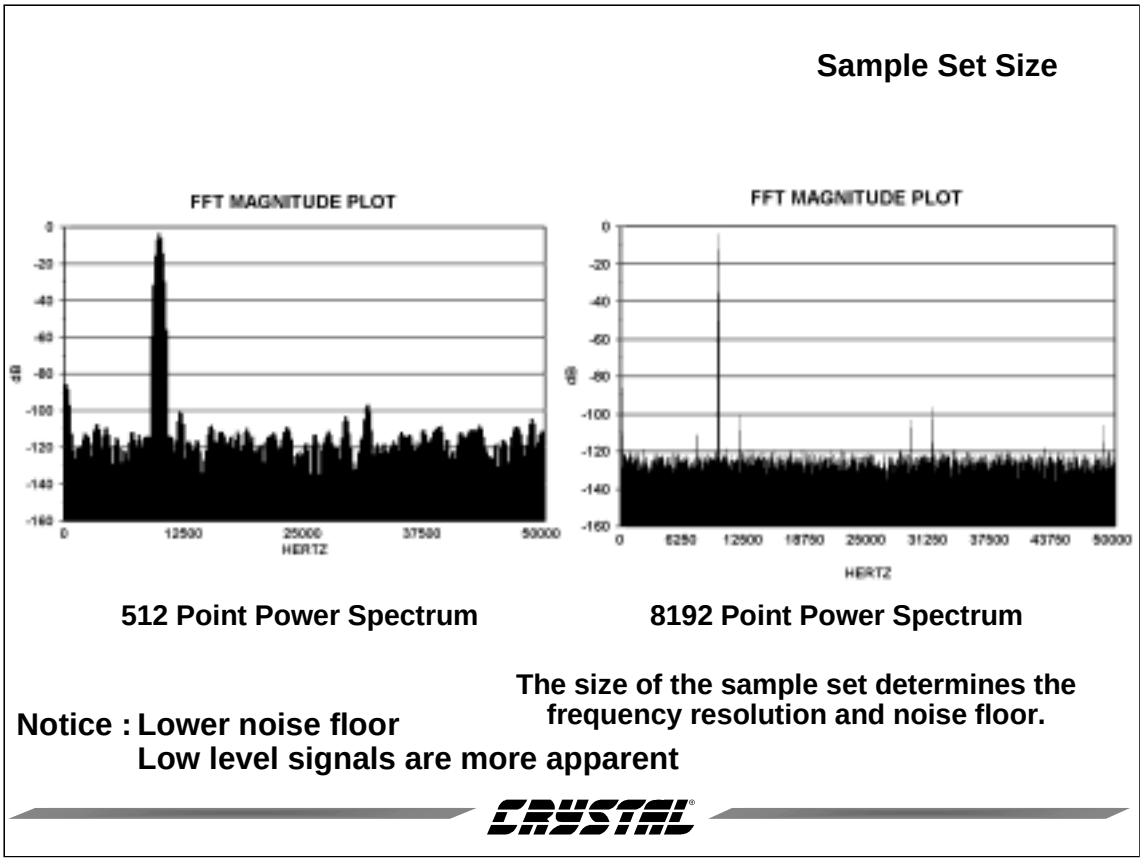
Total Harmonic Distortion is similar to SDR except the numerator and denominator are switched. THD is often used in audio applications as a measurement of linearity and is expressed either in terms of percentage (%) or decibels (dB).



Signal-to-Noise RATIO (SNR):

The Signal-to-Noise ratio is a measure of the broad band noise introduced into the signal. The noise corrupts dynamic signals, degrading accuracy at low voltage levels. The rms magnitude of the input signal is compared to the sum of the individual noise components. The ratio of the input signal to the sum of the individual noise components is expressed in terms of decibels (dB). The higher the SNR figure, the lower the broadband noise. The SNR number can be translated into effective bits.

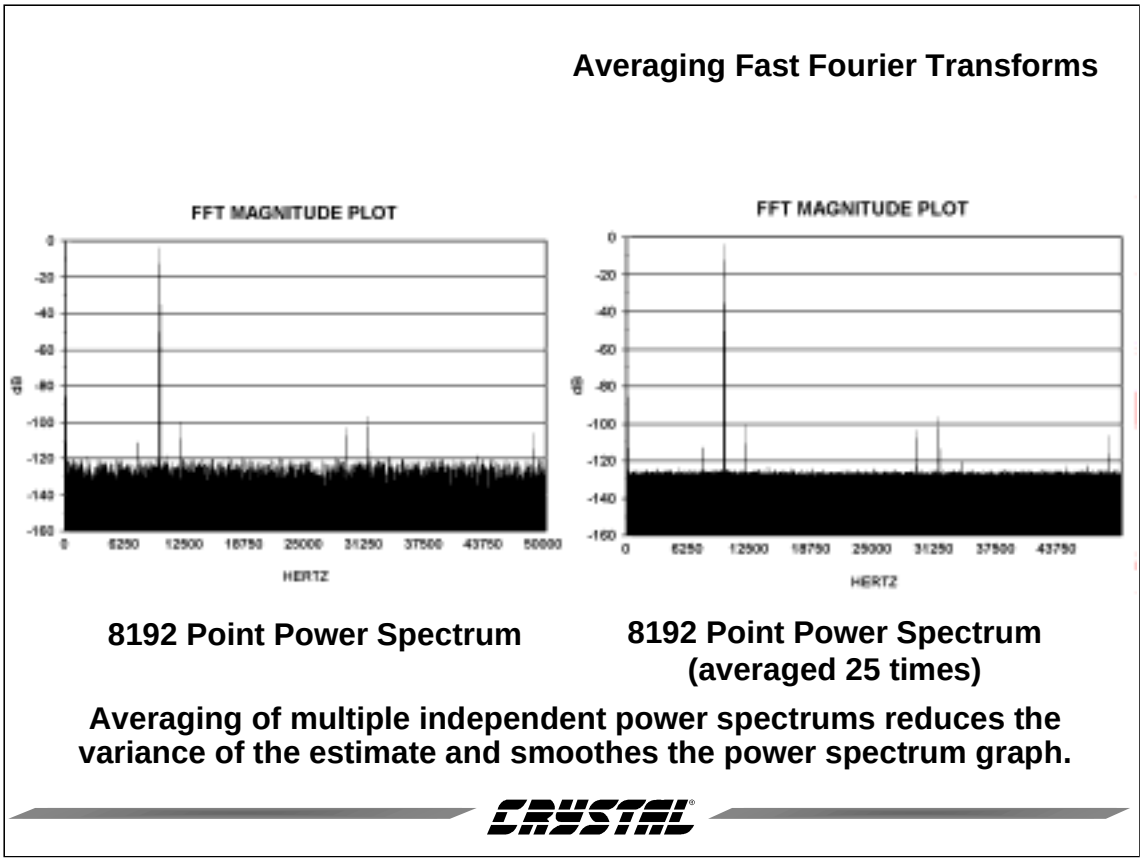
$$\text{Effective Bits} = \frac{\text{SNR} - 176\,\text{dB}}{6.02}$$



The size of the sample set used with the Fast Fourier Transform (FFT) algorithm determines the frequency resolution and the spot noise which makes up the noise floor. More information is contained in a large sample set than in a small sample set. An FFT of a large sample set uses the information to provide finer frequency resolution. The bin width is equal to the Sample Frequency divided by the number of samples (F_s / N). When sampling at 50 kHz, the bin width for a 512 sample FFT is 976.6 Hz and 61.0 Hz for an 8192 sample FFT.

Notice that the noise floor for the 8192 sample FFT is lower than the 512 sample FFT. The amount of total noise between 0 and 25 kHz is equal in both cases. But, the bin width for the 512 sample FFT is 16 times larger than the 8192 sample FFT. Since the bin is 16 times larger it will contain 16 times more broad band noise that is equally distributed across the spectrum. Thus the noise floor for the 8192 sample FFT should be 12 dB lower than the noise floor for the 512 sample FFT. With the lower noise floor, low level signals are more apparent.

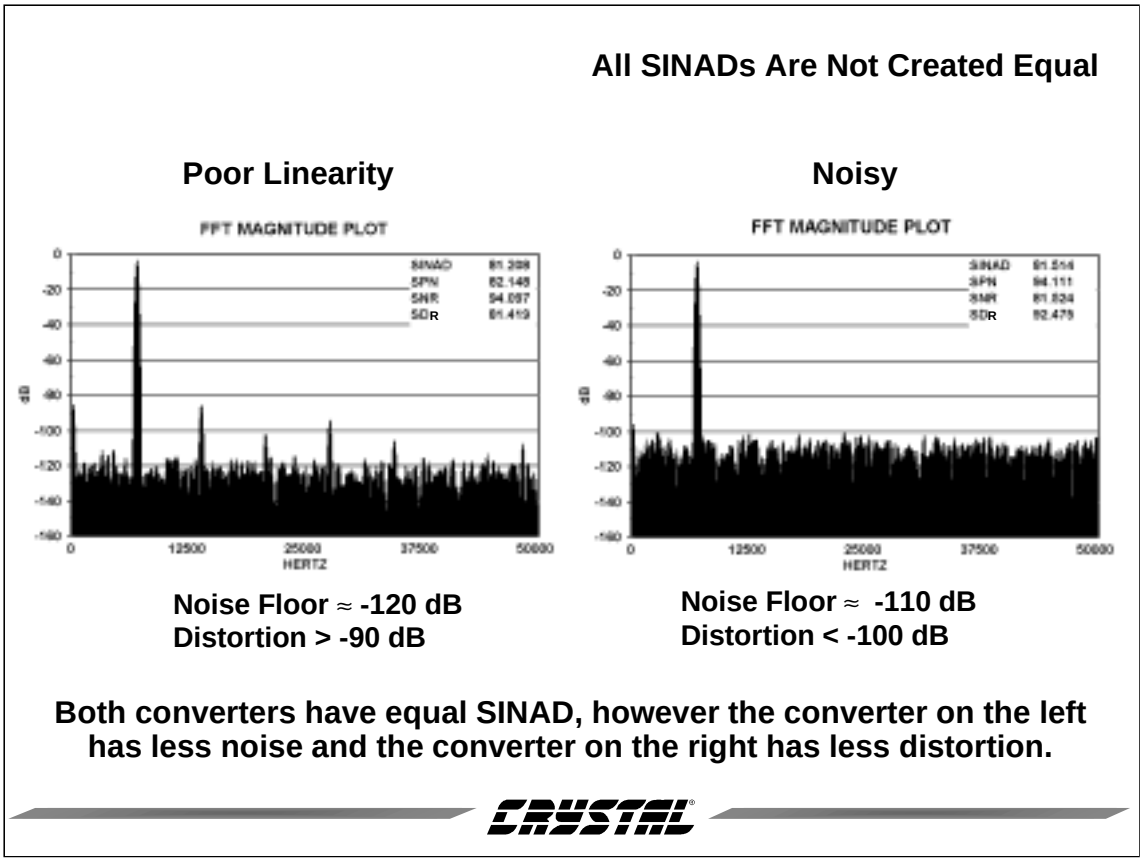
Energy levels at specific frequencies remain unchanged with the increase of sample size. The energy of a sinusoidal signal remains concentrated at a specific frequency. The energy associated with that specific bin will remain constant.



The power spectrums produced from an Fast Fourier Transform (FFT) use sampled data. The sampled data is a representative of the actual phenomena. The statistics calculated from sampled data only estimate the actual value, and have some uncertainty. Averaging multiple FFTs reduces the variances associated with the statistics calculated from sampled data.

Two power density functions are calculated, the first using one sample set, the second averaging 25 FFTs. In the power density function calculated from a single 8192 sample FFT, notice that the noise floor varies between -100 dB and -140 dB. The second power density function averages 25 FFTs in order to reduce the sampling uncertainty. The noise floor for the averaged FFT varies only by about 5 dB.

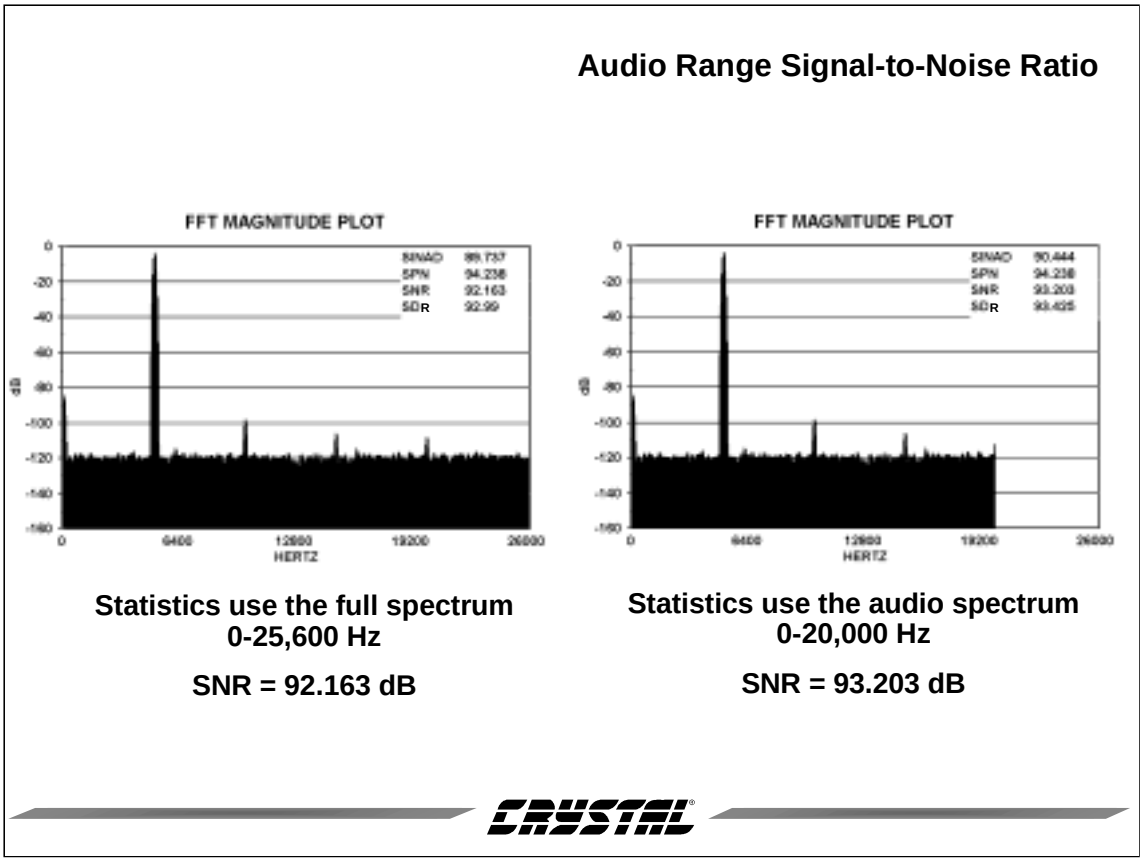
Averaging reduces the uncertainty of sampled data. Averaging multiple FFTs produces a smoother noise floor, making coherent noise easy to identify. The uncertainty due to random uncertainty is reduced by $1/\sqrt{n}$, where n is the number of samples averaged.



The Signal-to-Noise and Distortion (SINAD) figure is used as a measure for general purpose performance. The diagram to the left displays the power density spectrum for two different Analog-to-Digital Converters (ADC) which have identical SINAD values. Though the ADCs have identical SINAD values, they have distinctly different performance characteristics.

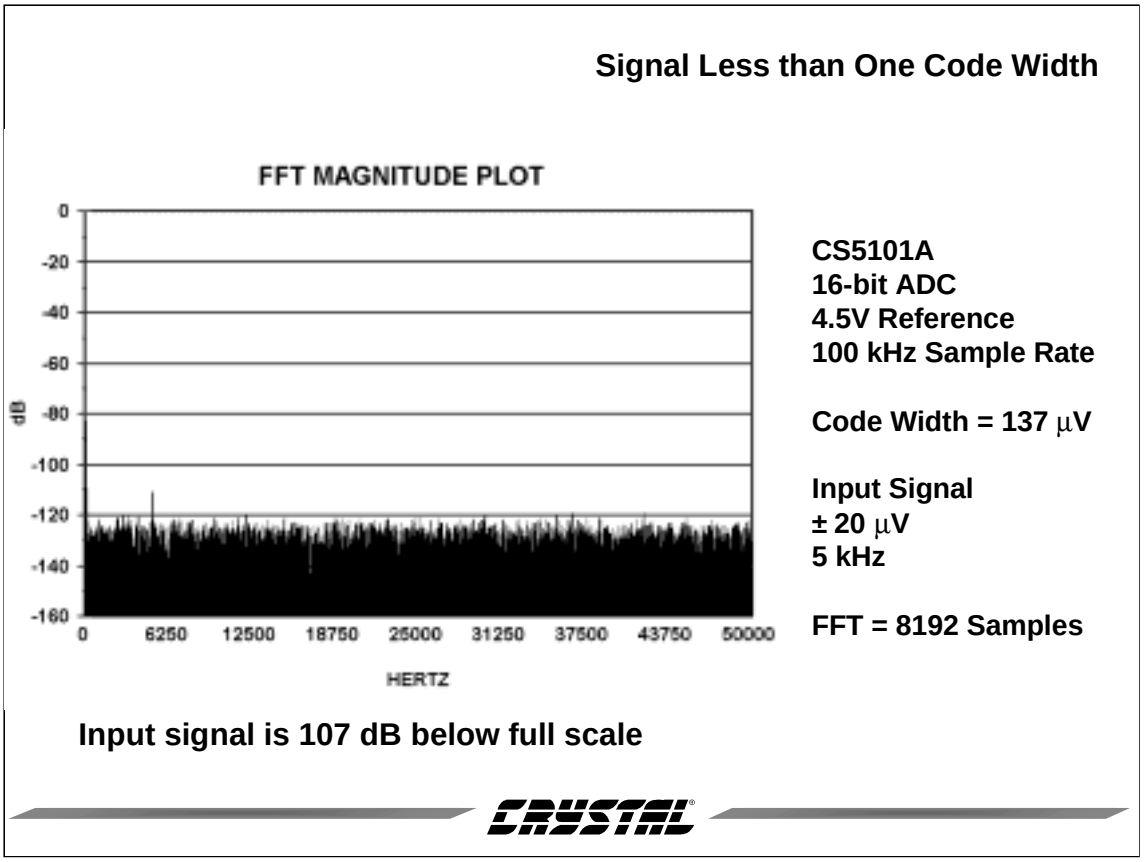
The plot on the left represents an ADC with poor linearity, which results in harmonic distortion. The Signal-to-Distortion (SDR) number is 81.419 dB. The Signal-to-Noise Ratio (SNR) number is very good at 94.097 dB. This ADC could be used in application where linearity is not important, such as measuring low level signals.

The other power density plot represents an ADC with high noise. The transfer function possess good linearity, represented by an SDR of 92.475 dB, however the SNR is 81.524 dB. This ADC could be used in application requiring low distortion.



Certain applications are interested in the dynamic performance within a specific frequency range. An Analog-to-Digital Converter (ADC) which samples at 51.2 kHz has a Nyquist frequency of 25.6 kHz. The signal statistics are normal collected using the energy between DC and the Nyquist frequency. The power density function on the left calculates its statistics using the spectral energy from DC to 25.6 kHz.

In an audio application the band of interest is up to 20 kHz. The spectrum of interest is less than the Nyquist frequency. The statistics in the second power density function use only the energy of the signals in the band of interest. Here, the Signal-to-Noise Ratio (SNR) below 20 kHz is 93.203 dB.

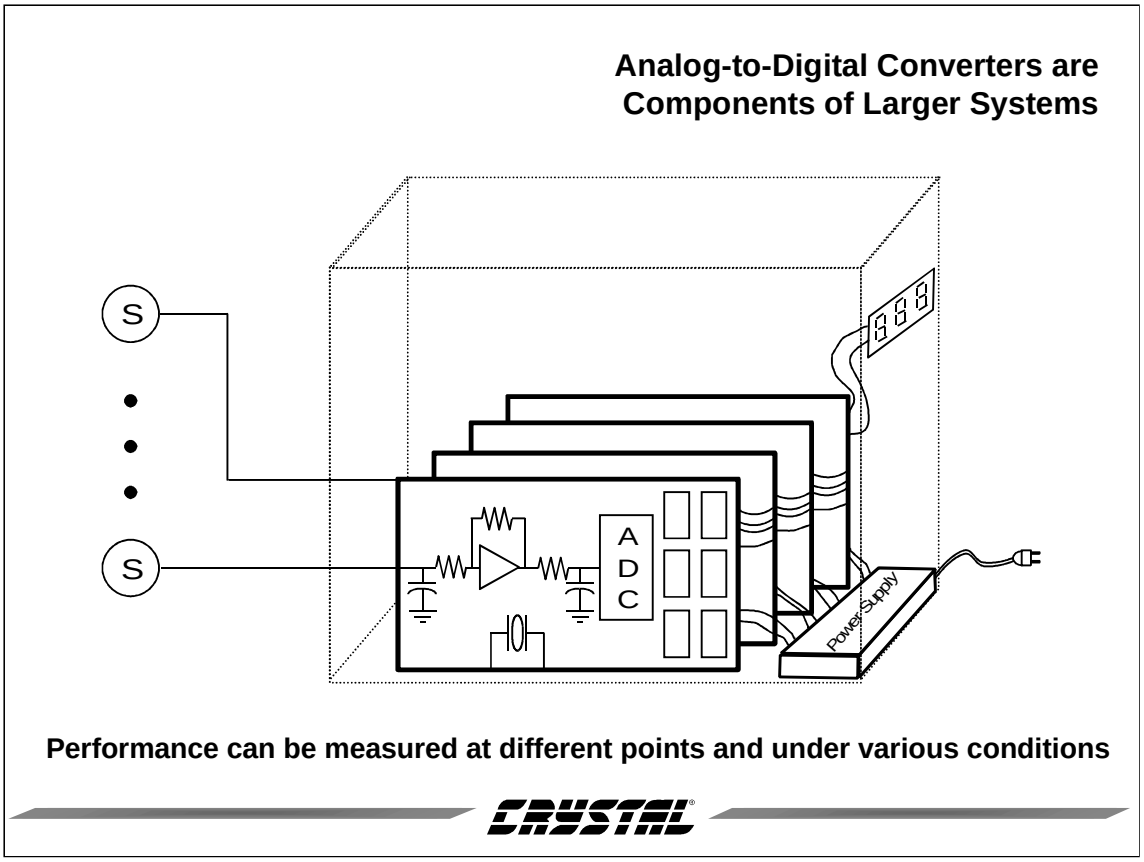


A common misconception is that a signal lower than the dynamic range cannot be detected nor measured. Using an ideal 16-bit Analog-to-Digital Converter (ADC), the theoretical best dynamic range is 98 dB. Signals that are more than 100 dB down from full scale can be detected.

In this example a Cirrus Logic Crystal CS5101A is used with a 4.5 volt reference, sampling at 100 kHz. The ideal code width for these conditions is 137 μV.

$$137\mu V = \frac{(+4.5V) - (-4.5V)}{2^{16}}$$

A 20 μV, 5 kHz signal is applied to the analog input. The 20 μV input signal is 107 dB below full scale. Using an 8192 sample FFT, the low-level 5 kHz signal is easily detected.

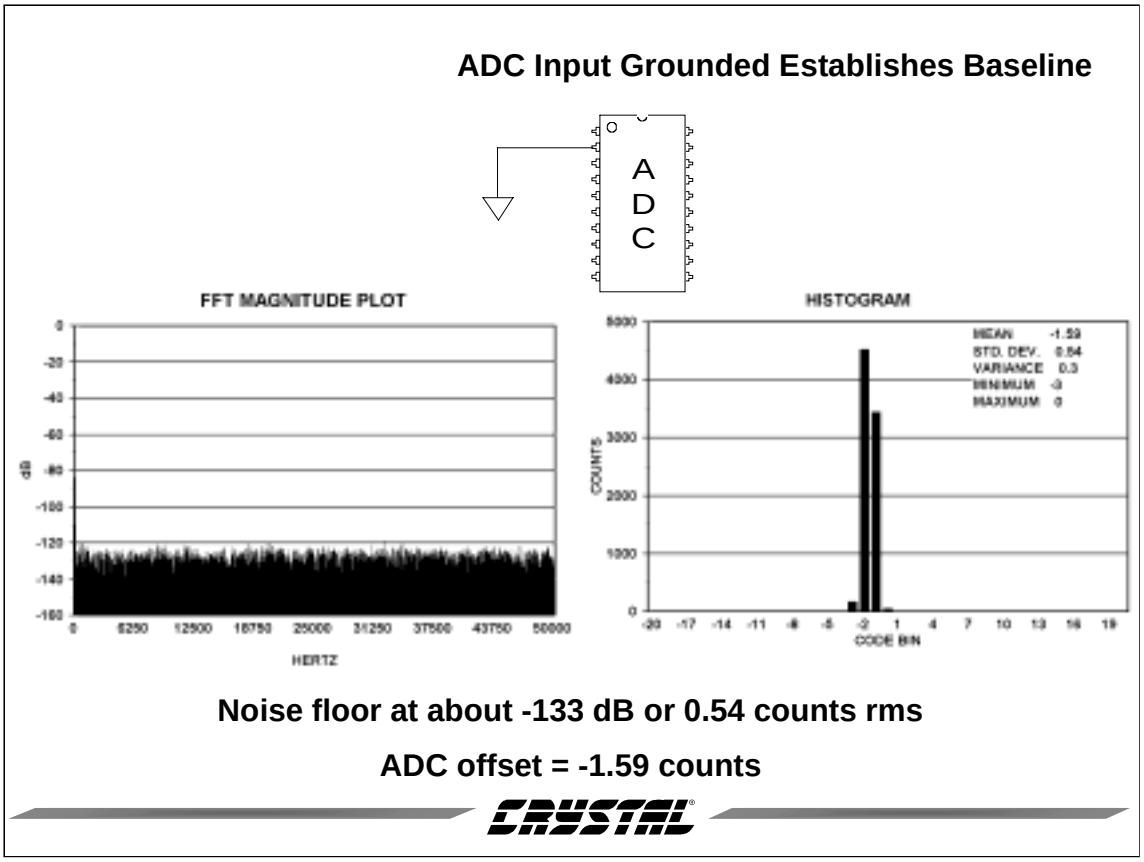


Analog-to-Digital Converters are components of larger systems which usually include analog and digital circuits, power supplies, electromechanical parts, wires, connectors and cables. Performance may be degraded as subsystems interact with one another.

Tests to quantify performance or troubleshoot a system can be made at different points in the system and under various conditions.

Tests applied to specific subsystems or components is used to isolate problems to a specific component or event.

One method to isolate problems is to measure the performance of basic subsystems to establish a baseline. The next step is to integrate the subsystems and measure the performance as integration progresses toward the completed system.

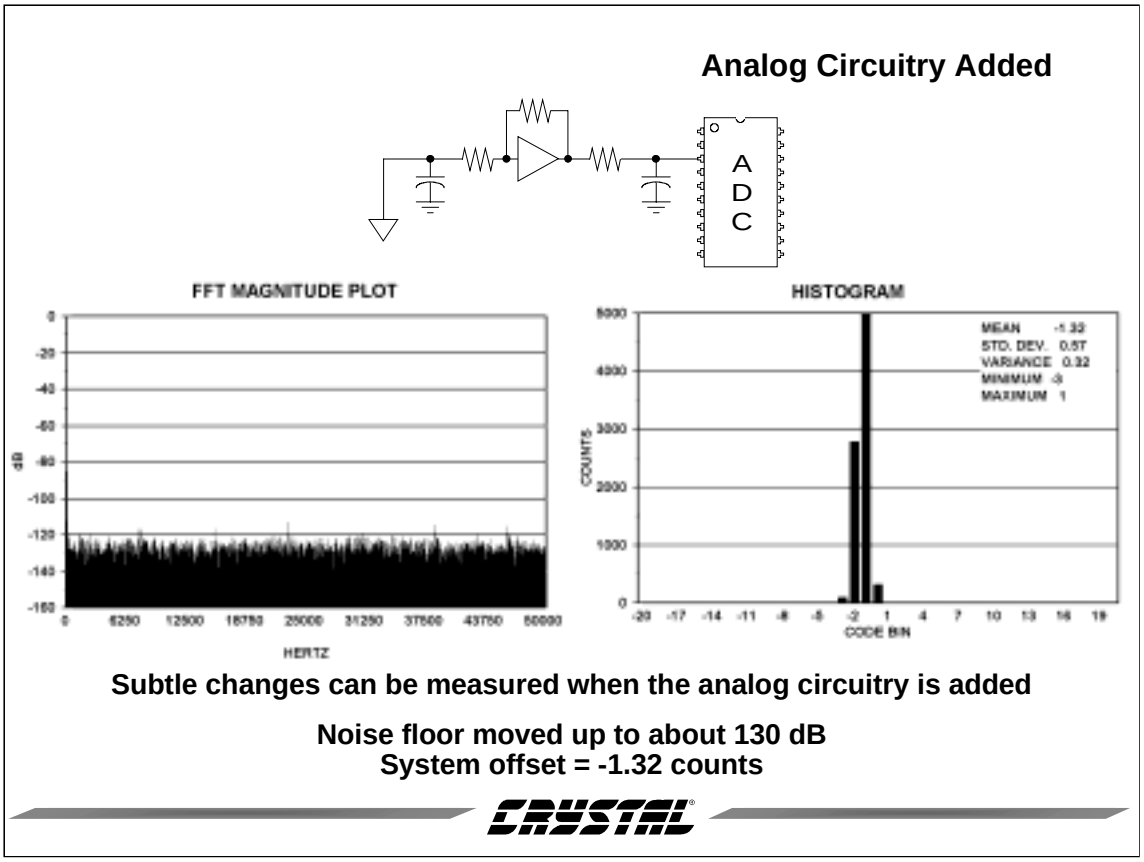


To establish a baseline for performance, the ADC is tested with a grounded input. One of the two tests performed on the collected data is a histogram and the other is an FFT. Each test provides different insight into the operation of the circuit.

With the grounded input, the FFT shows a flat noise floor which indicates that the noise is random and evenly spread across the frequency spectrum.

The histogram shows that the mean output from the ADC is -1.59 counts, indicating an offset of -1.59, and the standard deviation is 0.54, indicating an rms noise level of 0.54 counts.

As components are added to the ADC we can expect the offset to change and the rms noise to increase. If the changes are too severe, circuit modifications and improvements will have to be devised and implemented.



After some of the analog front end circuitry is added, the FFT and histogram tests are repeated and compared to the previous tests.

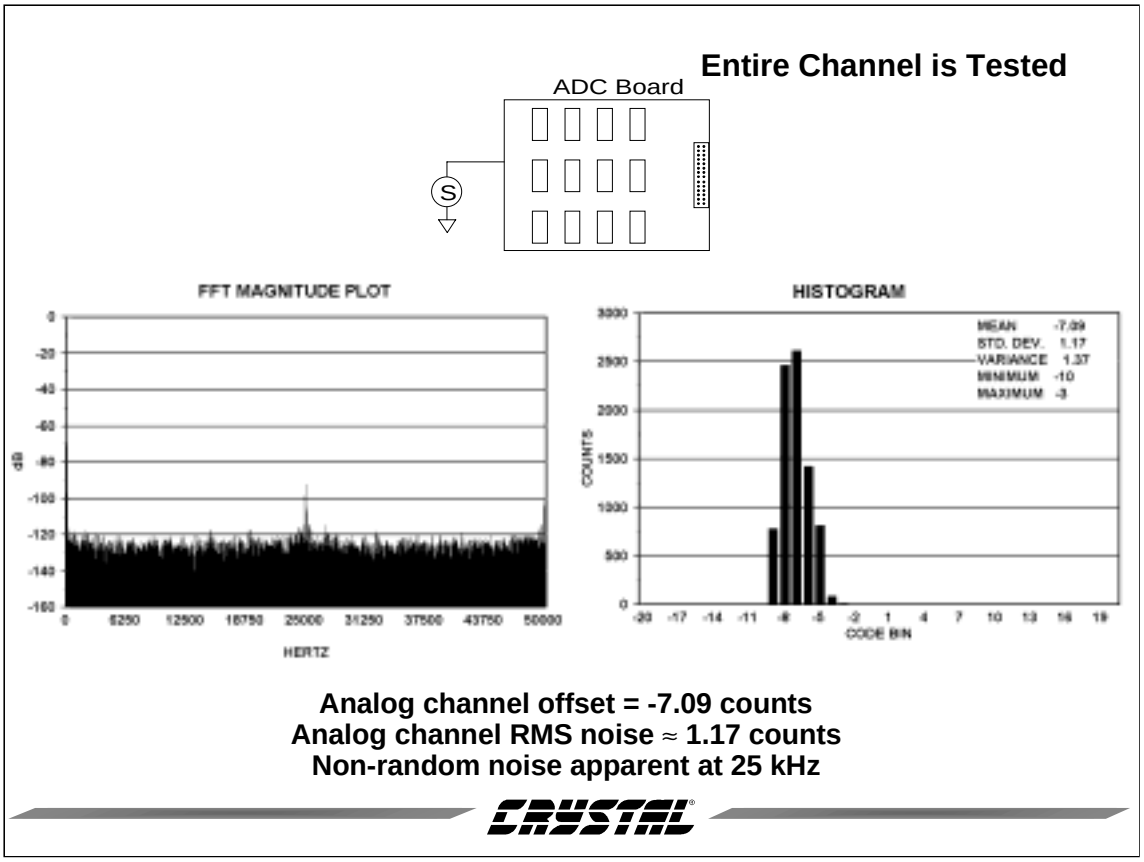
In the power density function display, small spikes of noise become apparent above -120 dB. This is an indication that some clock noise may be coupling into the analog circuitry. The level of the coherent noise is still fairly low. Notice that the noise floor has moved up to about -130 dB.

The mean change and the standard deviation increase in the histogram indicates a change in offset and added noise due to the components.

Recall that random noise voltages are added by taking the square root of the sum of square of the individual noise voltages.

$$\text{Total Noise} = \sqrt{V_1^2 + V_2^2 + V_3^2}$$

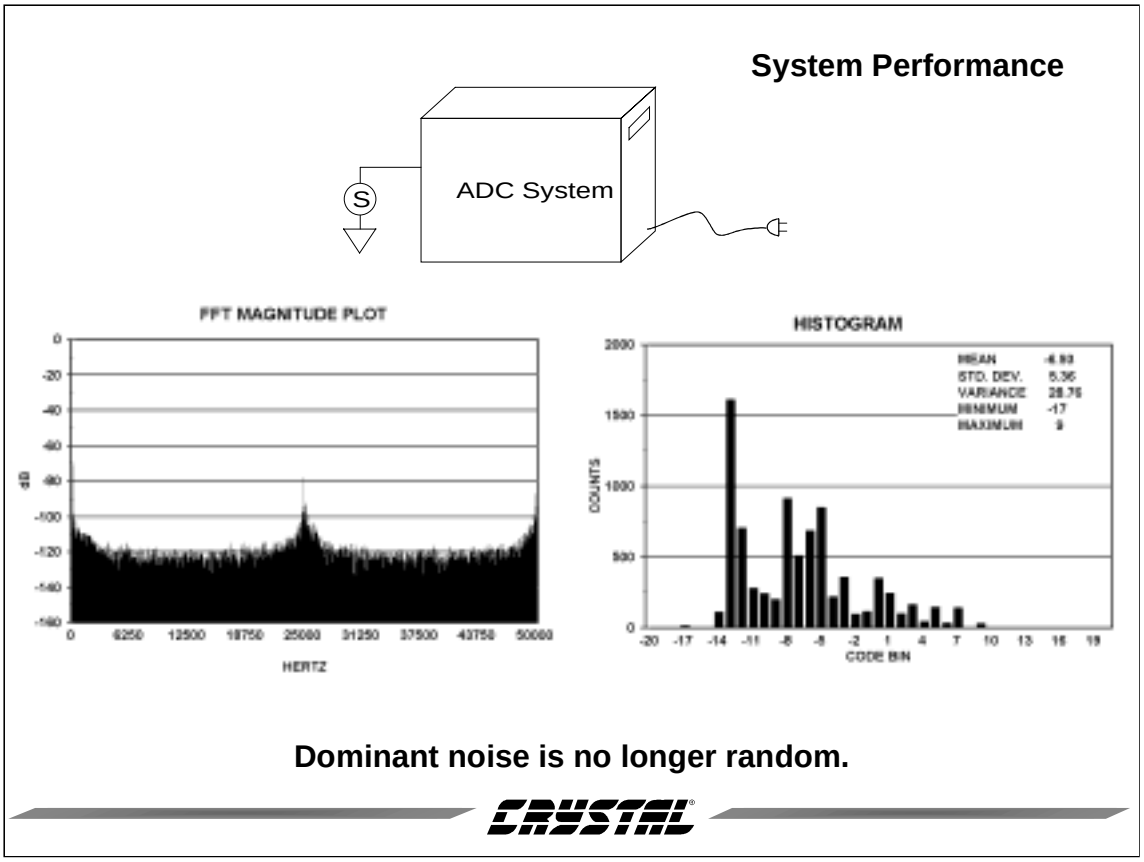
The overall changes in offset and noise are relatively small.



In this test the entire analog front end circuitry is added to the ADC. The sensor is set to its zero value and data is collected for an FFT and histogram.

In the histogram, the sample mean is -7.09 counts. This is the offset for the entire front end. The mean value can be stored and subtracted from the ADC readings to correct for the system offset.

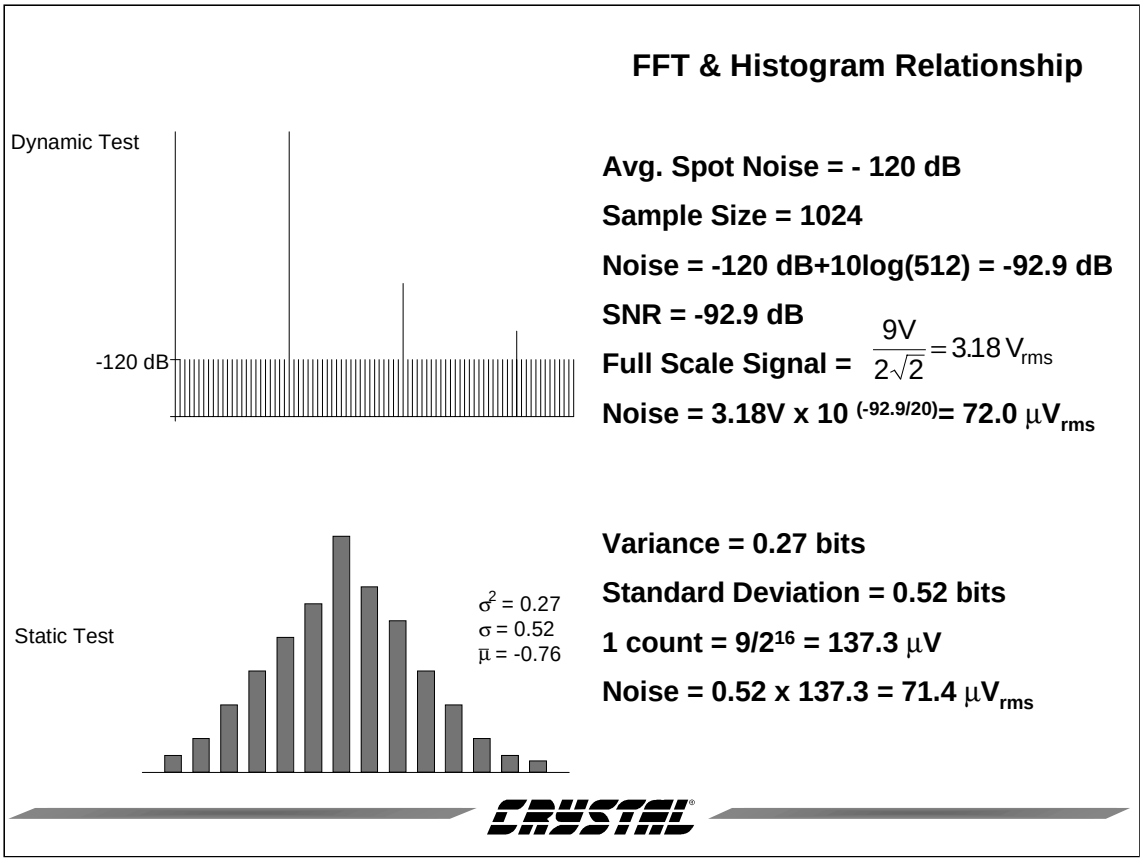
The FFT illustrates some surprising results. If just the histogram information were to be used, it might be assumed that the noise was entirely random. The histogram distribution appears to possess the familiar bell-shape. The power density function indicates that there is non-random noise at 25 kHz. Knowing the frequency of the noise, the source can be more easily located and the problem fixed.



The final test incorporates the entire system. Again the sensor is set to a zero value and a data set is collected. The tests now reveal that the dominant noise is no longer random.

The power density function indicates that there is significant noise at around 25 kHz, 50 kHz and DC. This noise could be from a switching power supply that is operating at around 25 kHz. This would produce noise at 25 kHz and at multiples of 25 kHz. High frequency noise could be aliased to lower frequencies.

An interesting test to implement would be to change the load on the power supply. An FFT could be used to see if the frequency and magnitude of the noise changes under different loading conditions.



When the noise is random, the FFT and histogram tests should correlate with each other. When looking at the power density function, a flat noise floor consists of random noise. The noise in the entire spectrum can be calculated by summing the noise power for each bin.

The power density function illustrated is created using 1024 samples. Thus the FFT has 512 bins (1024/2). Each bin is -120 dB below the full scale input. The noise power for all 512 bins is equal to -120 dB + 10 log(512) or -92.9 dB. In this example the calculations are easy with all 512 bin having the same value, however this method can be used to estimate the noise floor by estimating the power density function.

The rms value of a full scale signal is :

$$\text{Full Scale Signal} = \frac{9V}{2\sqrt{2}} = 3.18\,V_{rms}$$

The noise is 92.9 dB less than 3.18 volts or 72 μV rms.

The variance of a histogram is 0.27 counts which translates to a standard deviation of 0.52 counts. The bit size is determined by the input span and the ADC resolution. In the case of a 16-bit ADC with a 9 volt input span, a bit is equivalent to 137.3 μV.

From the histogram, the noise is estimated as being 0.52 counts or 71.4 μV rms.

Thus the rms noise calculated from the power density function is 72 μV and 71.4 μV using a histogram.

Applications Reference Guide - Section IV

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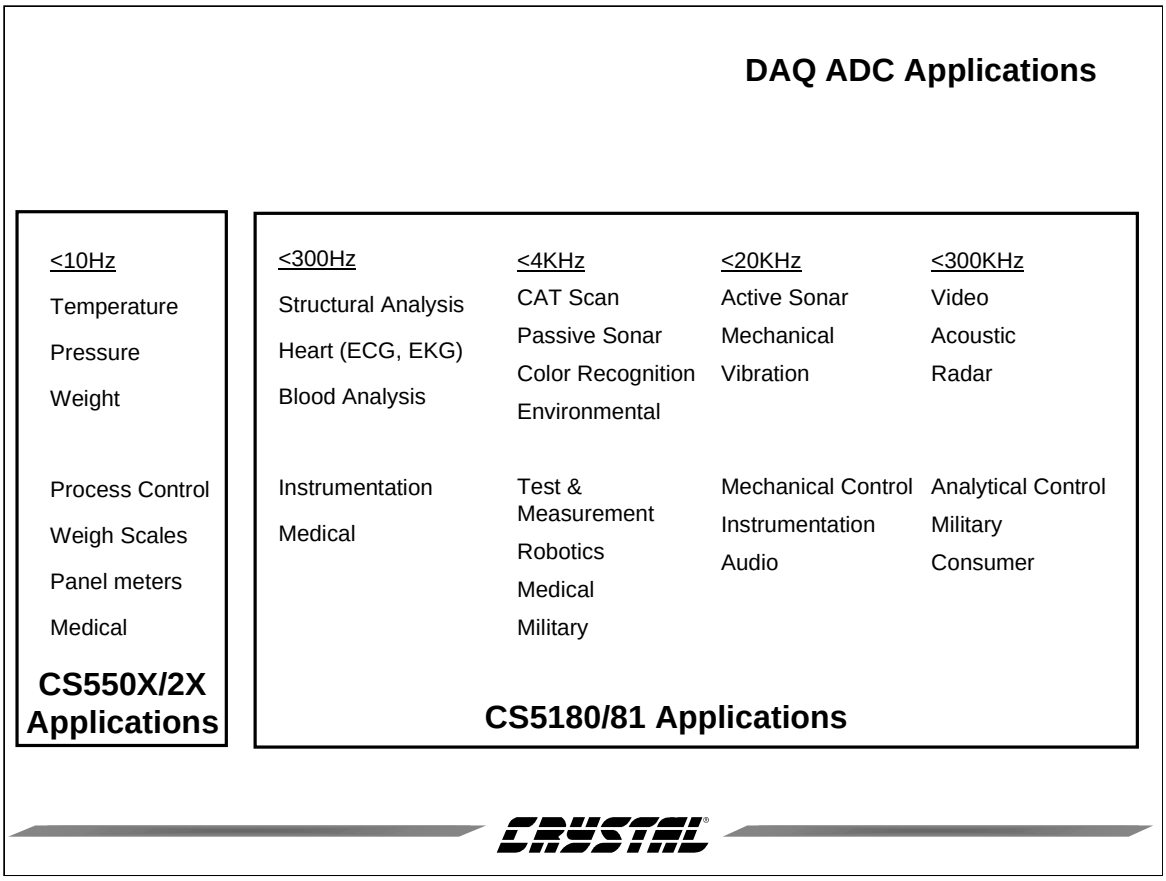
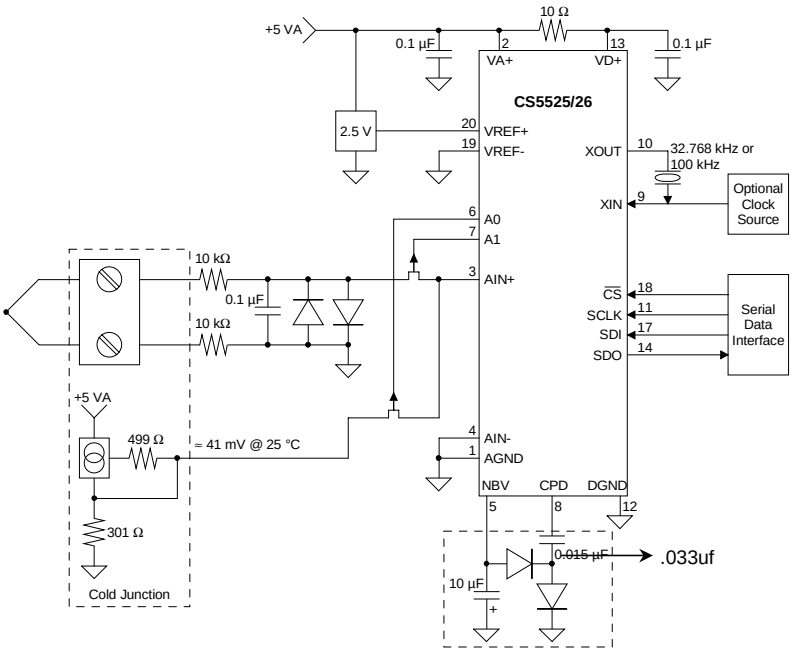
- **Technical Support Services**

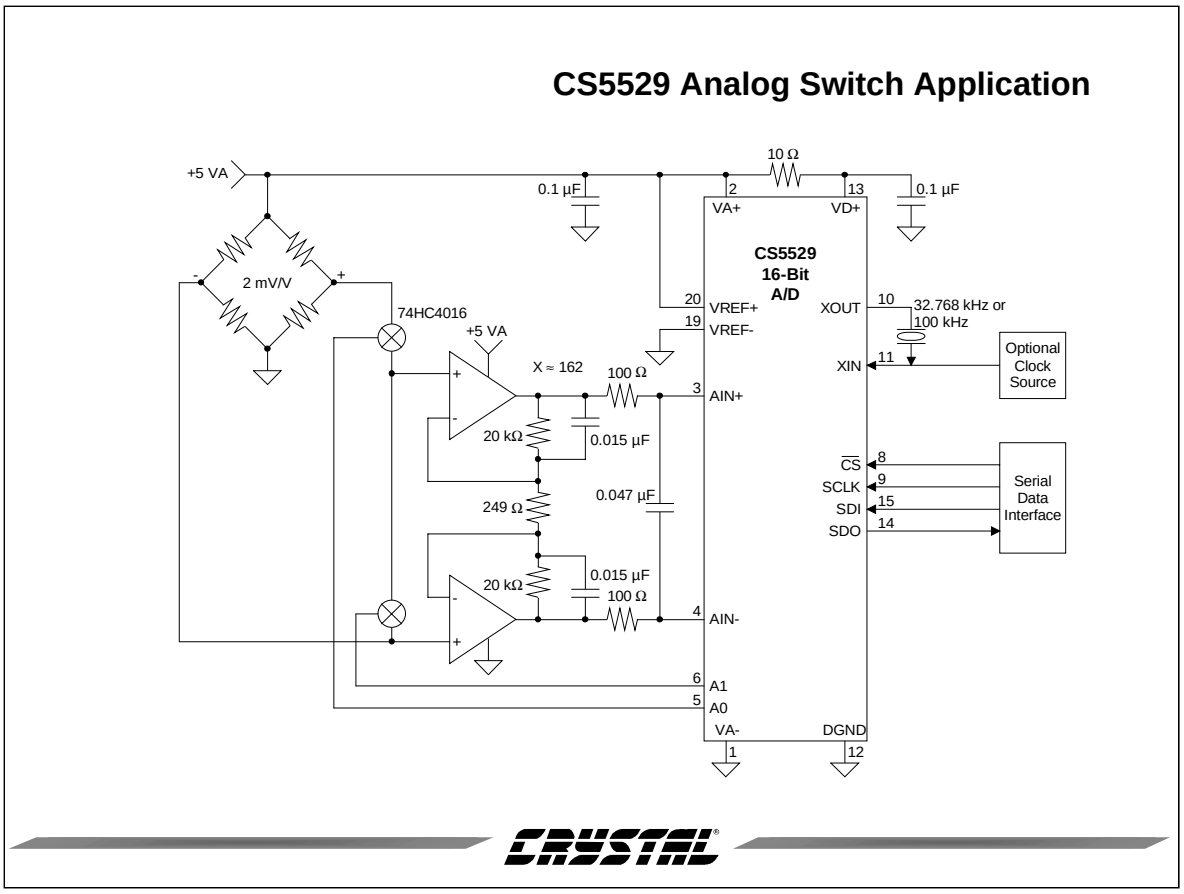


Data Acquisition applications span a variety of frequency ranges. Low frequency application such a temperature, pressure, and medical applications can utilize the CS552x family. Higher frequency application such as acoustic, radar, and sonar can use the CS5180/81.

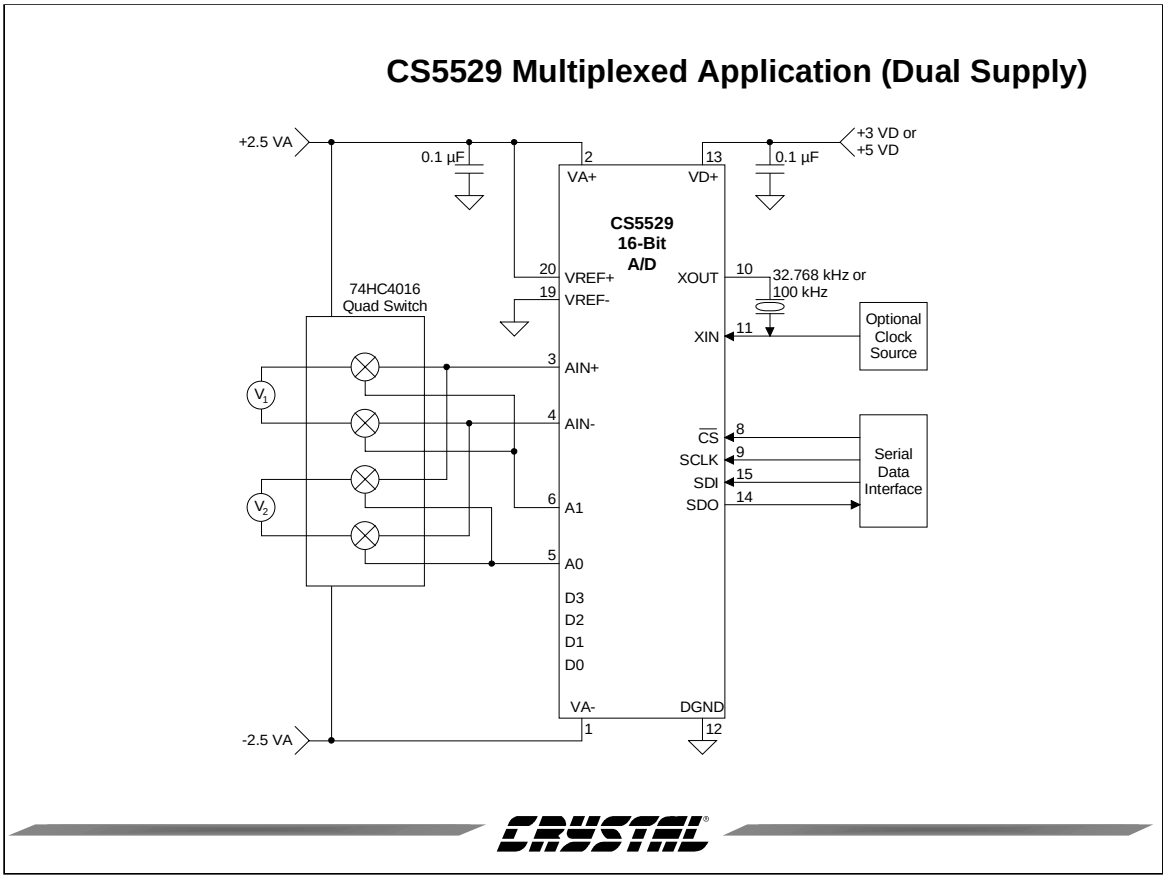
CS5525/26 Thermocouple Application Circuit



The circuit above uses the CS5525/26 in a thermocouple measurement application. To accommodate ground referenced signal and to eliminate a negative supply, the circuit uses the CS5525/26's charge pump drive. Two J-177 P-channel switches were added to accommodate the cold junction channel.

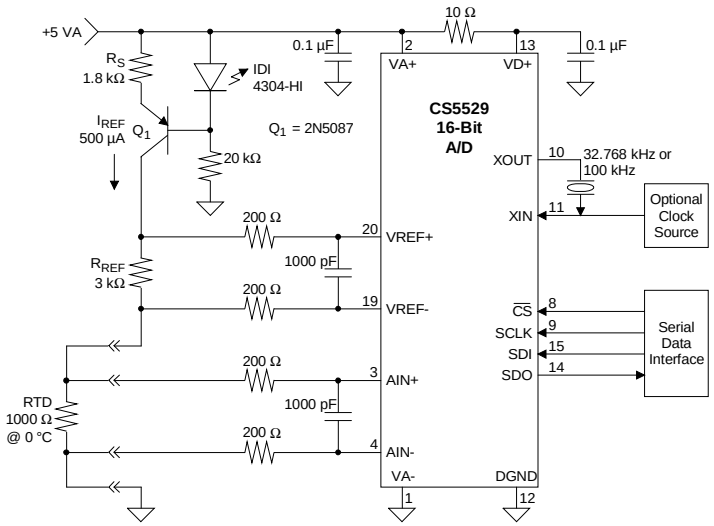


The CS5529's analog switches, A0 and A1, can be used to short the inputs of external amplifier to accommodate system offset calibration. The switches can then be bypassed to accommodate full scale system calibration.



The CS5529 offers a 6 bit output latch. Two bit are powered from the analog supply and 4 bits are powered from the digital supply. The analog powered latch bits were designed to accommodate analog switches such as the 74HC4016 which require a supply to supply transition to turn to the switch off or on. The digital powered latch bits were designed to accommodate multiplexers which only require to 0 to 5 V transition. The latch can accommodate two analog switches and a 16-channel multiplexer.

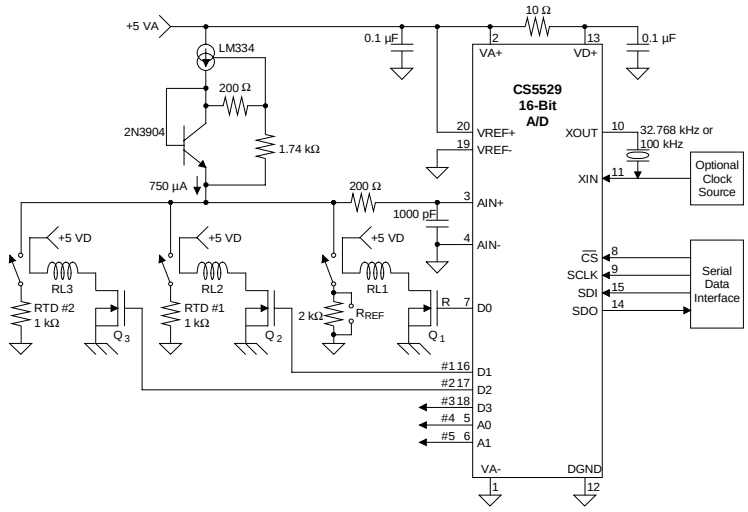
CS5529 Ratiometric RTD Application



RTD Digitizer provides 80 Counts/°C over -200 to 550 °C

The circuit above uses the CS5529 in a ratiometric RTD application. The current source in the circuit generates approximately a 500 µA current and provides first order temperature compensation with the IDI4304-HI diode. A 1.5 V reference is generated as the current flows through the 3 kΩ reference resistor, Rref. The current then excites the 1000W RTD. Since the analog input signals from the RTD and the voltage reference input are excited from the same current source, any variation in the current will cause a proportional change in the RREF and the RTD. This configuration eliminates any errors due to power supply or current source variations.

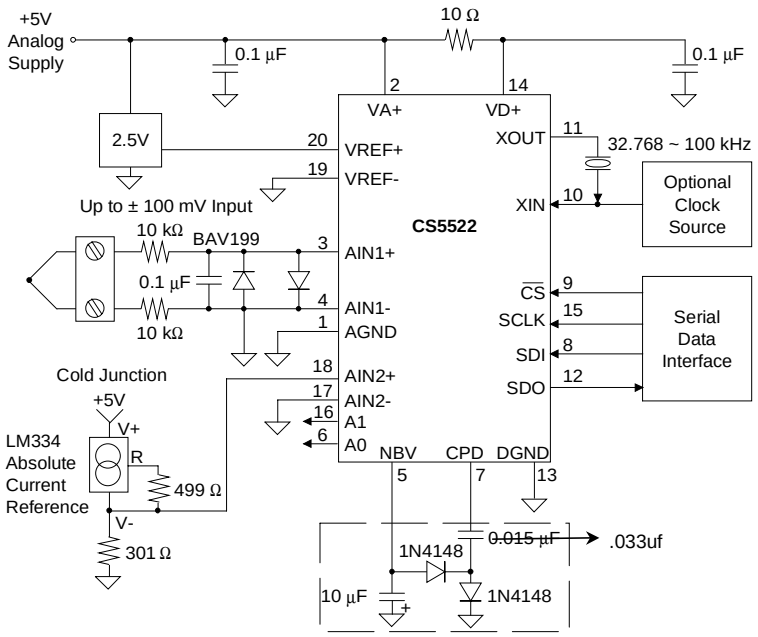
CS5529 Multi-channel Ratiometric RTD Application



Multi-channel RTD Digitizer Ratios Sensor Resistance against a Reference Resistor (R_{REF}) to Measure -200 to 550 °C

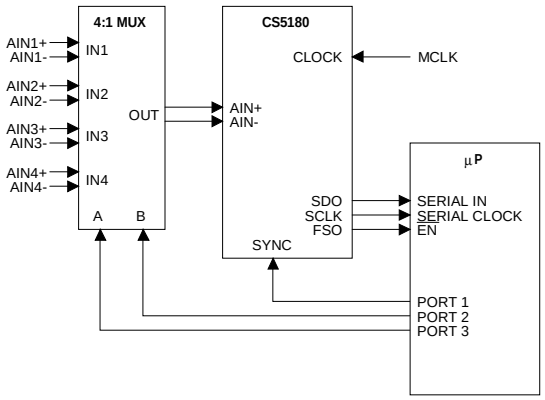
The circuit above uses the three of the digital outputs of the CS5529 to select one of three resistors. The circuit uses two measurements to ratio. The resistance of one of two RTDs against the 2K reference resistor. Accuracy is a function of the 2K resistor and the output impedance of the current source.

CS5522 Thermocouple Application



The circuit above uses the CS5522 in a thermocouple measurement application. To accommodate ground referenced signal and to eliminate a negative supply, the circuit uses the CS5522's charge pump drive. The circuits also uses the CS5522's multiplexer to accommodate the cold junction channel.

Using the CS5180 With Multiplexed Inputs

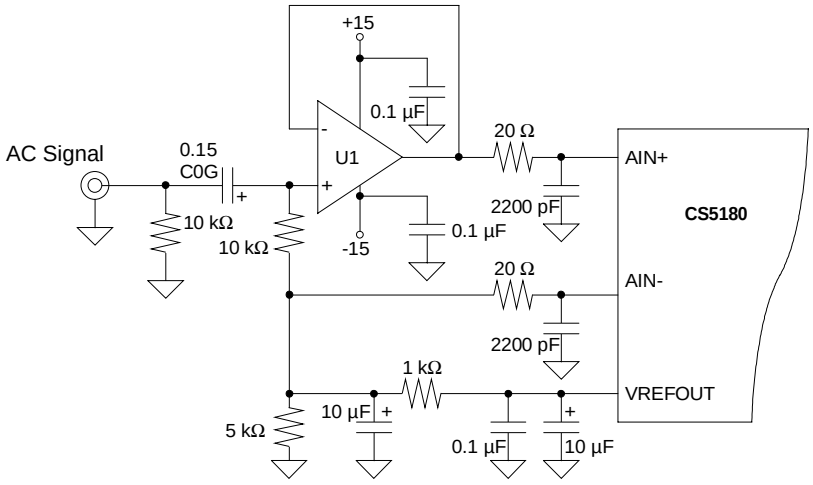


(User must allow adequate time for CS5180 internal filter to settle after switching channels)

Typical 4-Channel Data Acquisition System

Example shown is a 4-channel data acquisition system. User must allow adequate settling time for the internal filter to settle after switching channels.

CS5180 Input Signal Conditioning



A single op-amp can be used to feed a capacitively coupled, ground referenced signal into the CS5180 AIN+ input while also stepping up the common mode voltage into the required range of 1.0 Volts to Vref+0.25 Volts.

Driving the CS5180/81 for AC applications:
The circuit shown uses a single op-amp to drive the inputs of the CS5180 from a capacitively coupled, ground referenced signal source. Vref is used to bias up the inputs into the required range of 1.0 to Vref + .25 VDC.

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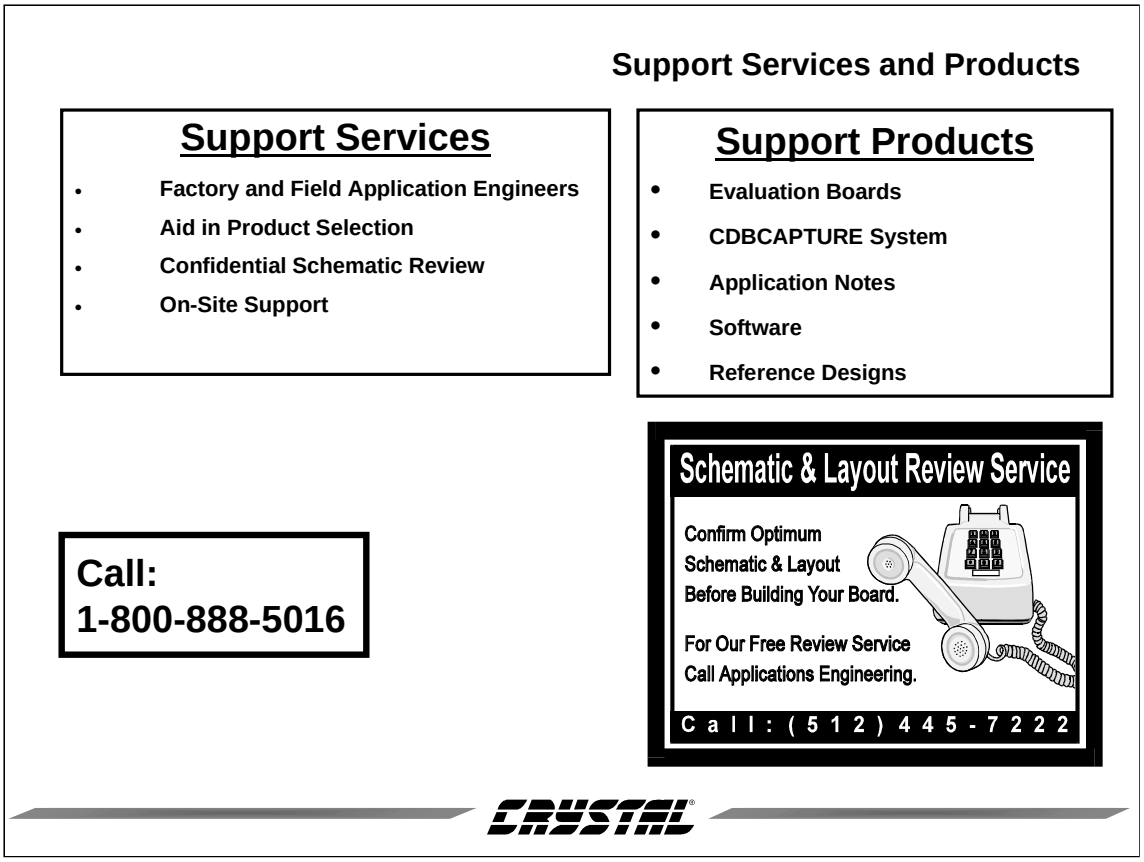

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Acronyms

Analog-to-Digital Converter	**ADC**
Delta Sigma	**ΔΣ**
Differential Nonlinearity	**DNL**
Digital Signal Processor	**DSP**
Digital-to-Analog Converter	**DAC**
Discrete Fourier Transform	**DFT**
Fast Fourier Transforms	**FFTs**
Integral Nonlinearity	**INL**
Least Significant Bit	**LSB**
Most Significant Bit	**MSB**
Phase Locked Loop	**PLL**
Probability Density Function	**PDF**
Radio Frequency Interference	**RFI**
Signal-to-Distortion Ratio	**SDR**
Signal-to-Noise and Distortion	**SINAD**
Signal-to-Noise Ratio	**SNR**
Signal-to-Peak-Noise	**SPN**
Silicon-Controlled Rectifier	**SCR**
Small Outline IC	**SOIC**
Successive Approximation	**SAR**
Total Harmonic Distortion	**THD**
Voltage Controlled Crystal Oscillator	**VCXO**
Voltage Controlled Oscillator	**VCO**